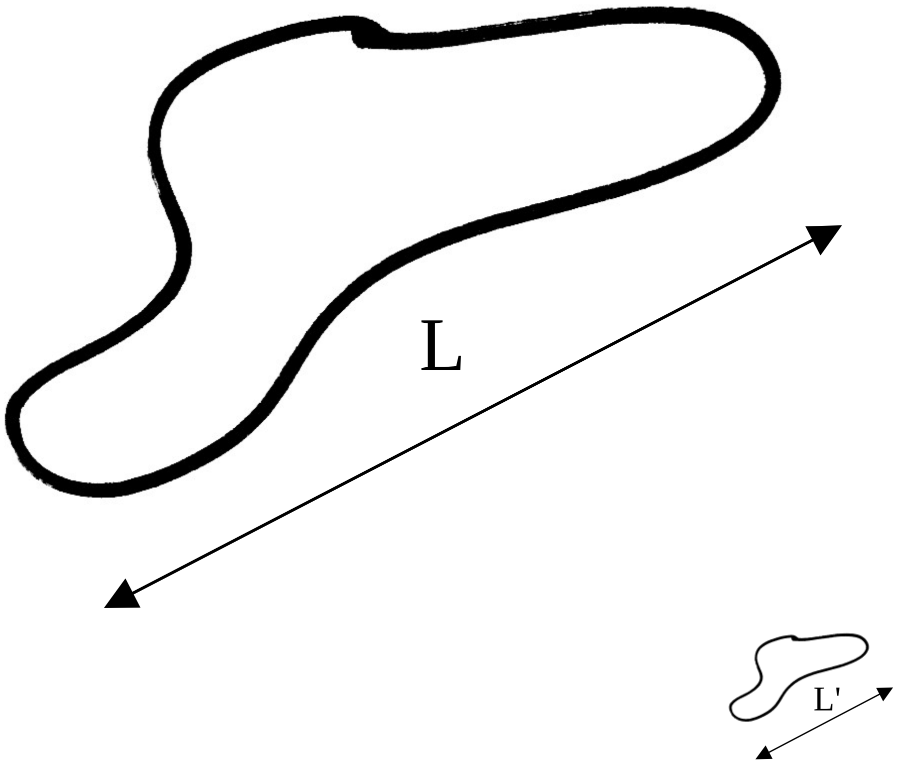
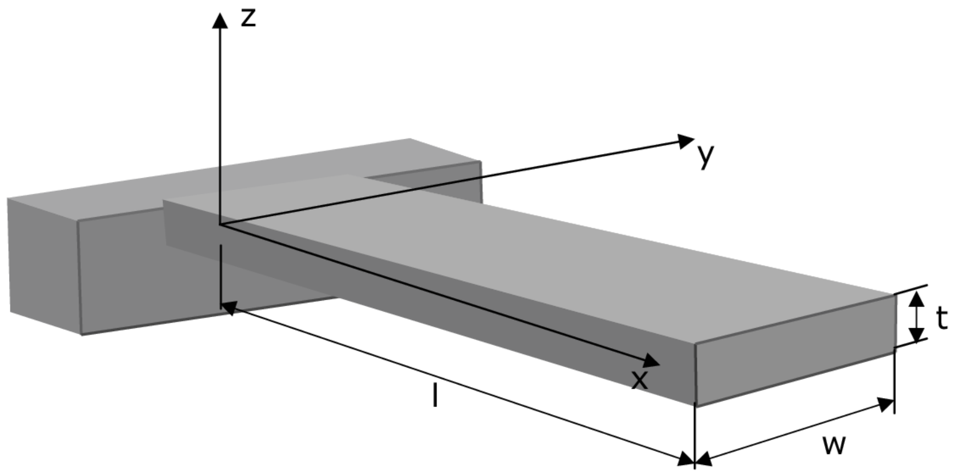
Advanced MEMS and Microsystems

Dr. Danick Briand, Prof. Guillermo Villanueva, Prof. Niels Quack, Dr. Sebastian Gautsch

Bonus lesson – Scaling laws intro



$$L^* = \frac{L'}{L}$$



$$m^* = \ell^{*3}$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{m}}$$

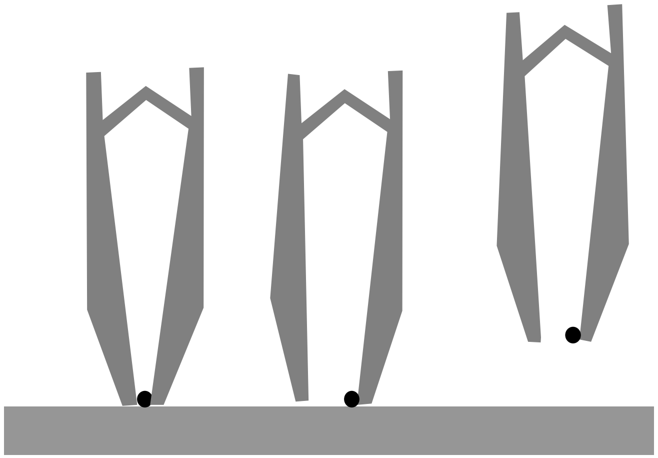
$$k = \frac{3EI}{L^3}$$

$$I = \frac{bh^3}{12}$$

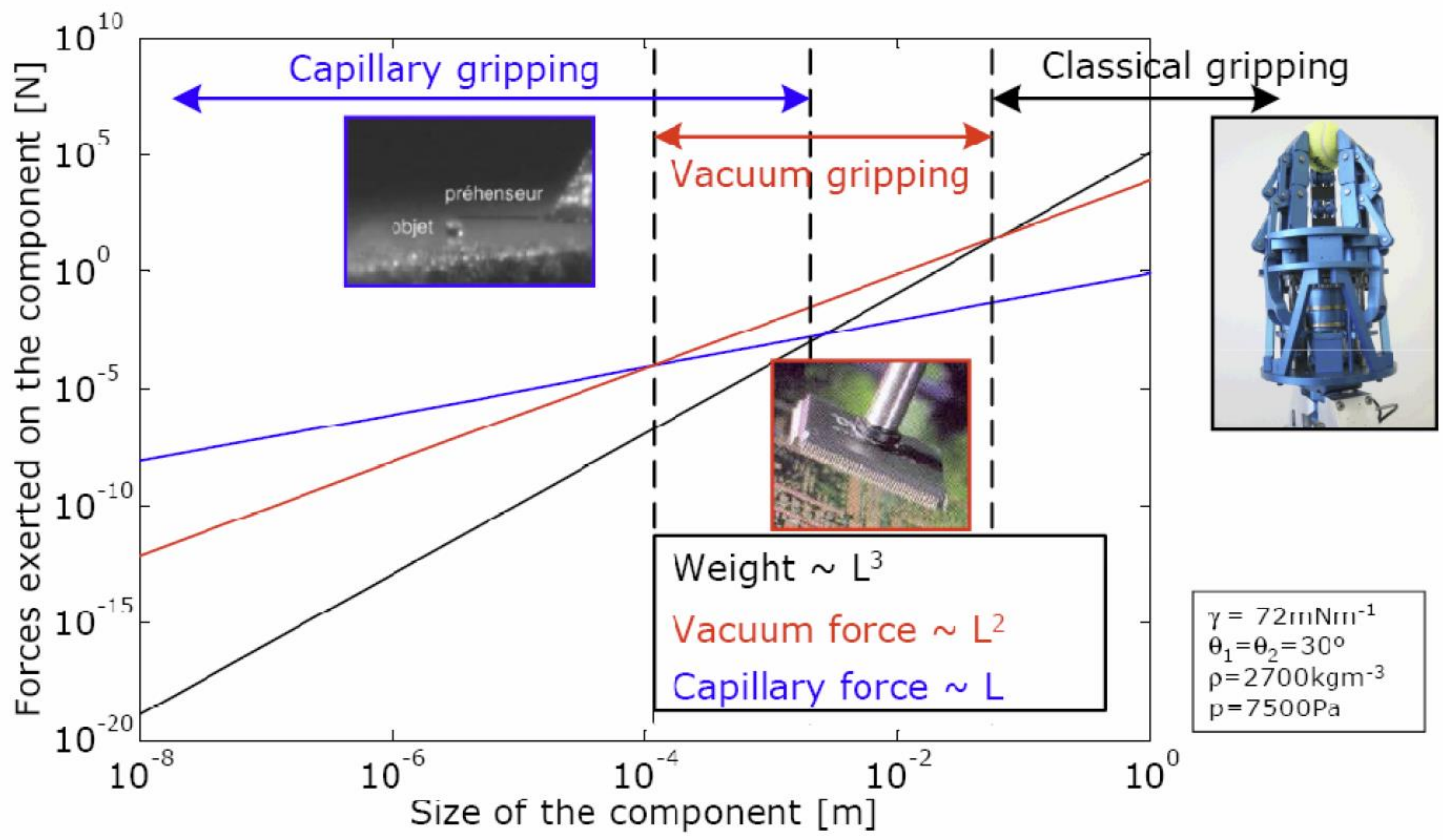
$$f_0^* = \sqrt{\frac{k^*}{m^*}} = \frac{1}{\ell^*}$$

$$k^* = \frac{\ell^{*4}}{\ell^{*3}} = \ell^*$$

- Dominant physical phenomena are different from those of the macro world
- Adhesive forces (van der Waals force, electrostatic forces, surface tension) are more dominant than gravity in microworld



MEMS intro: Scaling laws



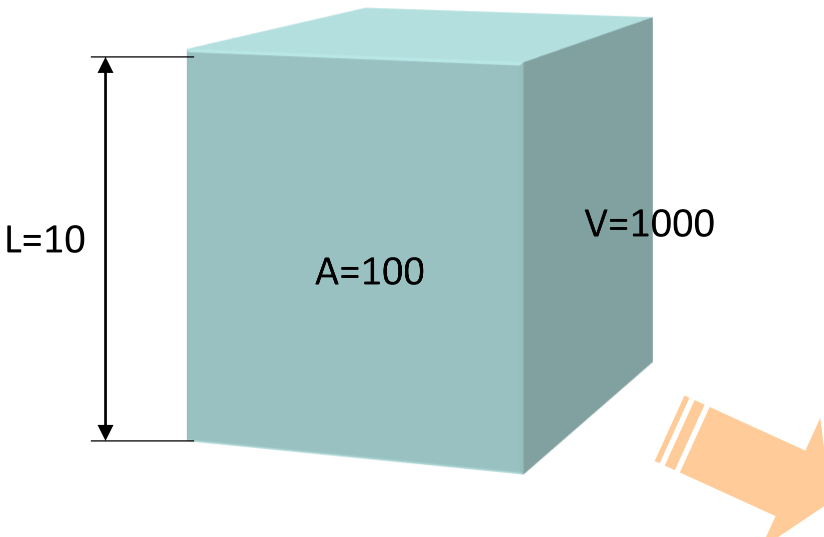
Sources de g. à d: Haliyo03, vangastel04, Université de Laval

Surface to volume ratio:

Calculate the surface to volume ratio of two cubes whose sides are 1mm and 10mm, respectively.

Diffusion:

calculate the time that a drop of milk takes to diffuse across a cup of coffee (diffusion in one dimension, no stirring, with $D = 10^{-9}\ m^2/s$)

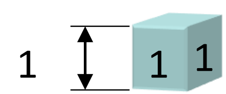


Scaling of dimensions

- length l
- area l^2
- volume l^3

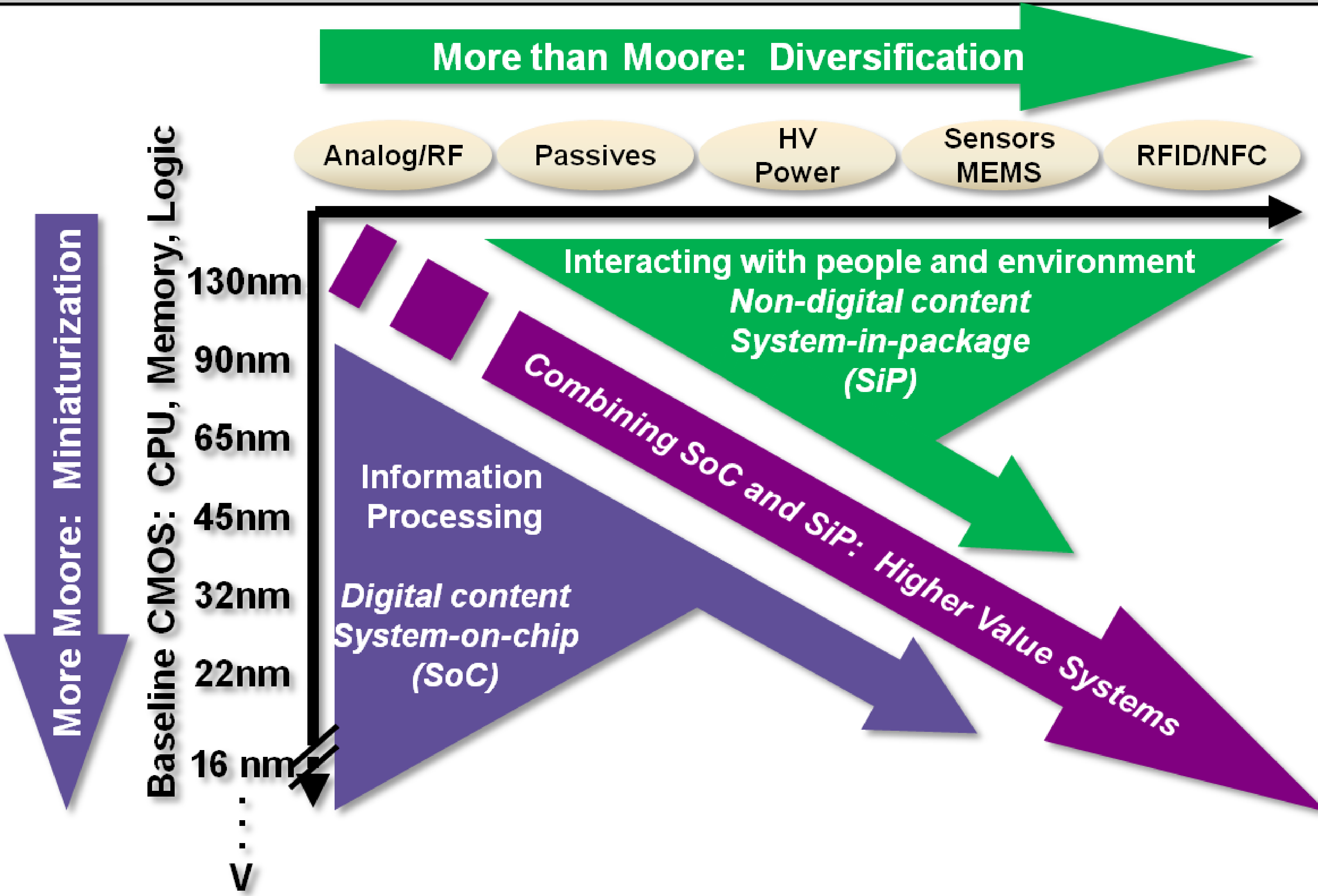
Diffusion (Fick's 2nd law):

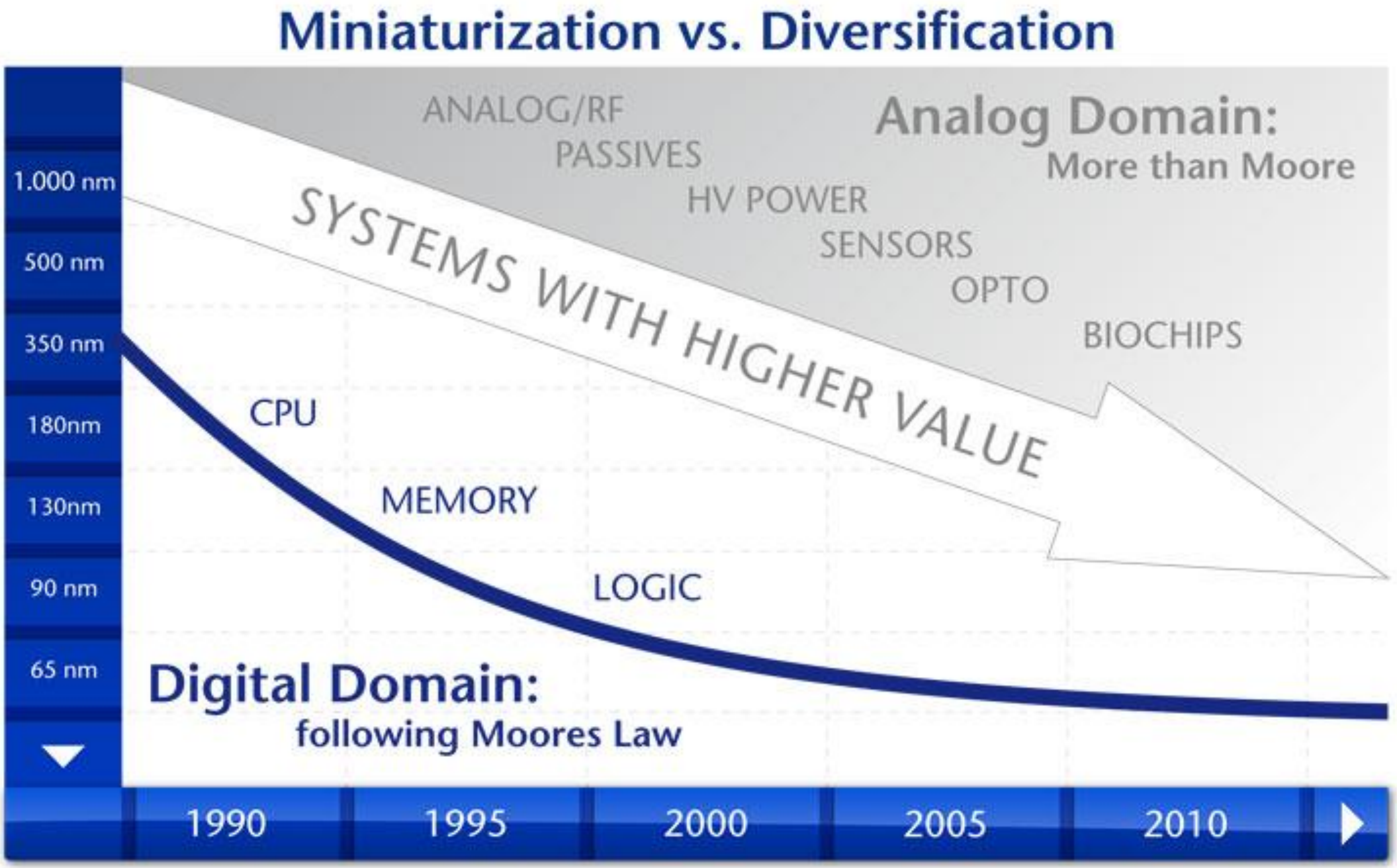
- $x = \sqrt{2\,D\,t}$



Dimension (mm)	*Volume*	*Surface-volume ratio*	*Diffusion time (s)*	*Number of molecules conc. of 1mM*
1	1 mL	1	500	6×10^{11}
0.46	100 nL	2	107	6×10^{10}
0.22	10 nL	4	23	6×10^{9}
0.1	1 nL	10	5	6×10^{8}
0.05	100 pL	22	1	6×10^{7}
0.02	10 pL	46	0.2	6×10^{6}
0.01	1 pL	100	0.05	6×10^{5}
0.001	1 fL	1000	0.0005	602

MEMS intro: Moore's law




Miniaturization vs. Diversification
ANALOG/RF
PASSIVES
HV POWER
SENSORS
OPTO
BIOCHIPS
Analog Domain:
More than Moore
SYSTEMS WITH HIGHER VALUE
1.000 nm
500 nm
350 nm
180nm
130nm
90 nm
65 nm
CPU
MEMORY
LOGIC
Digital Domain:
following Moores Law
1990
1995
2000
2005
2010

Bonus lesson – Microfabrication

Lecture content

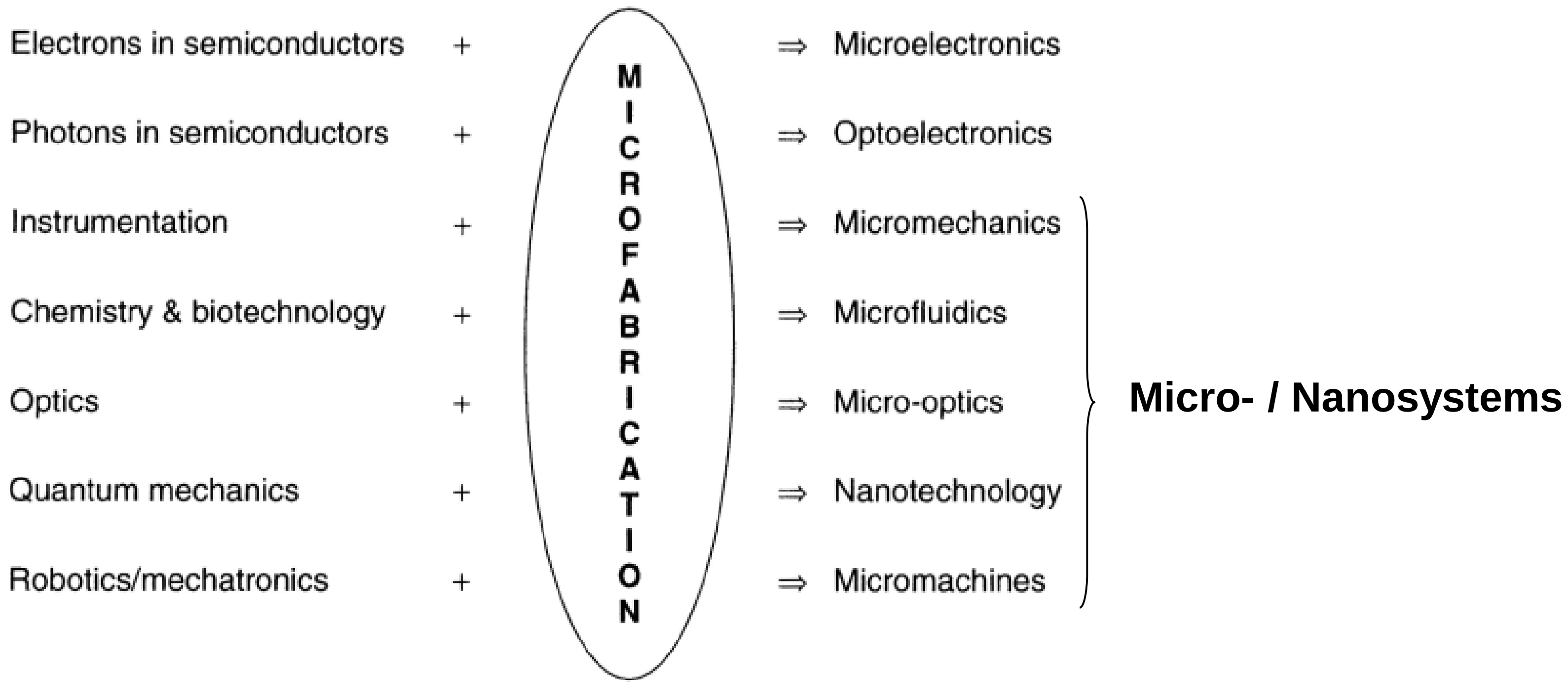
1. **Introduction**
   - Cleanroom facilities
   - Silicon bulk material
2. **Lithography**
   - E-Beam
   - Pattern transfer
3. **Bulk Micromachining**
   - Isotropic wet etching
   - Anisotropic wet etching (KOH),
   - Isotropic Dry etching (RIE)
   - Anisotropic Dry etching (DRIE)
4. **Surface Micromachining**
   - Thin film depositions techniques, PVD, CVD, electroplating, …
   - Poly-SI, sacrificial layer techniques
5. **Other techniques**

For More details:

From G.T.A. Kovacs, Micromachined Transducers Sourcebook, 1998 M. Madou, Fundamentals of Microfabrication, 1997

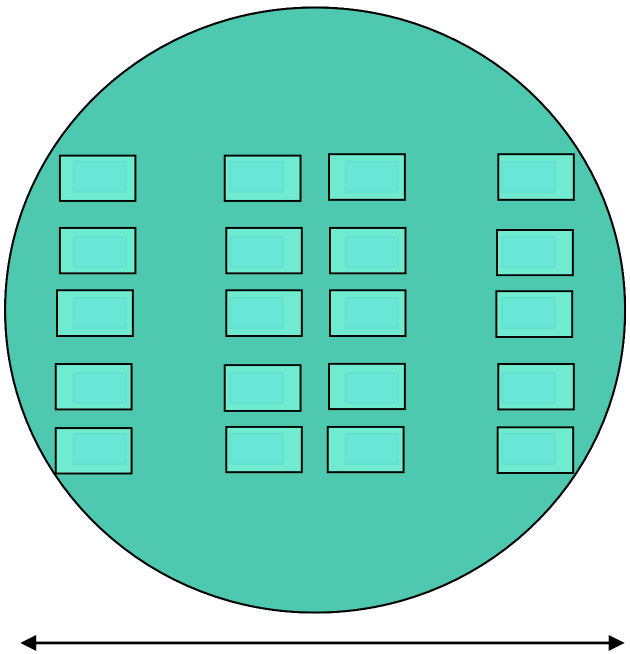
Youtube Video lecture series: *http://www.youtube.com/watch?v=JJElLA8k6Qg&list=PLWbWYEQLbAEaN1VdH9KF1G3TPQE06AbWd*

A manufacturing technology for making microscopic devices (ICs, MEMS) and benefits of the properties linked to the small dimensions



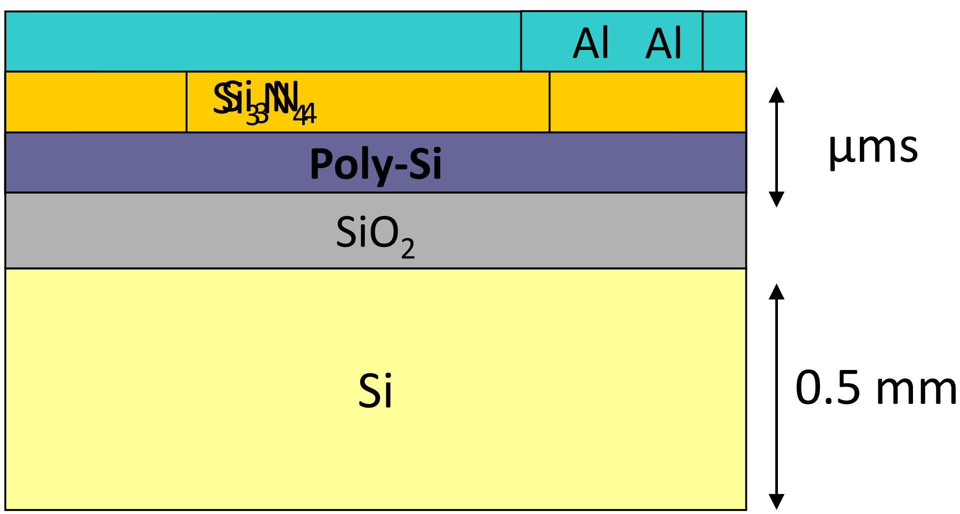
From S. Franssila, Introduction to Microfabrication, John Wiley & Sons Ltd (UK)

- Based on successive steps of thin film deposition and patterning
  - more than 20 steps in the ICs industry, Films thickness: 10 nm - few µms

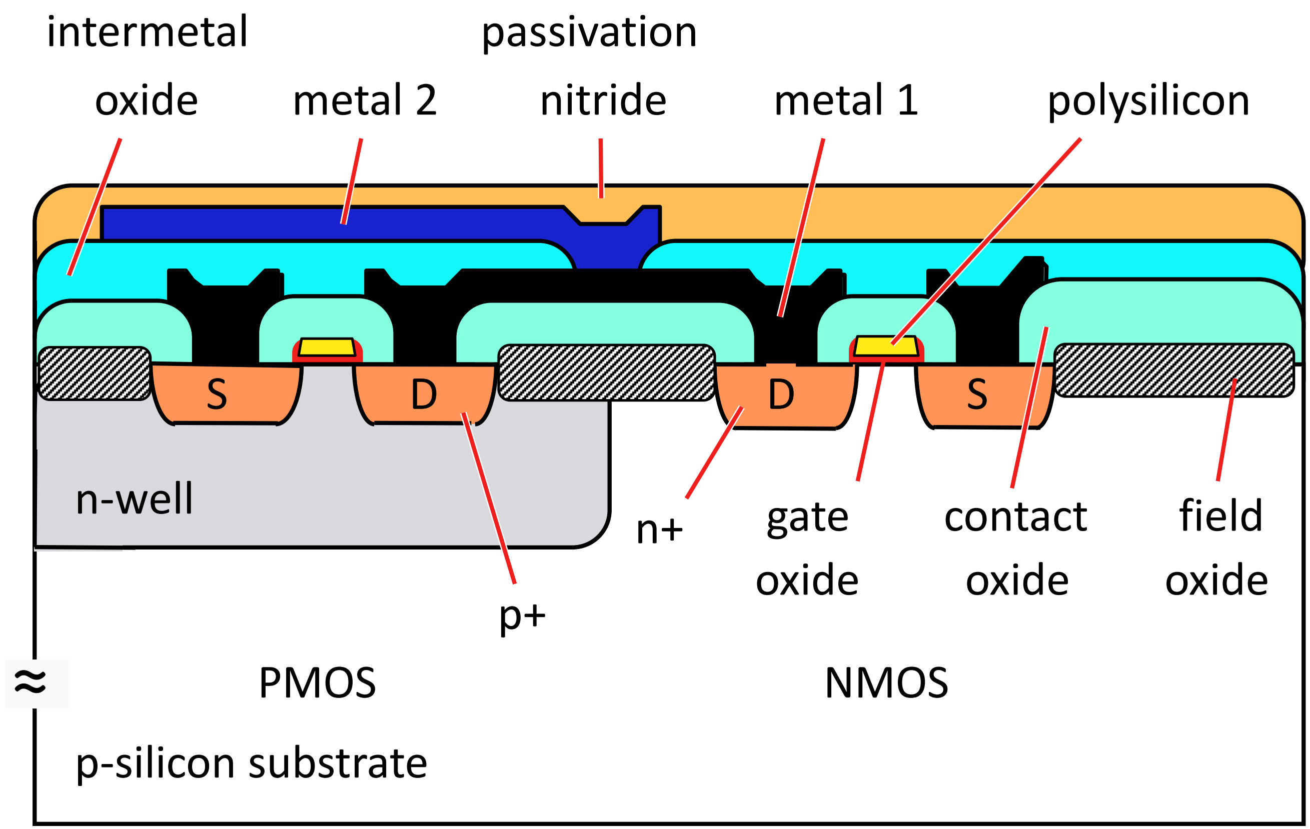


100 to 300 mm

Example: Poly-silicon resistors



Microfabrication – CMOS Process

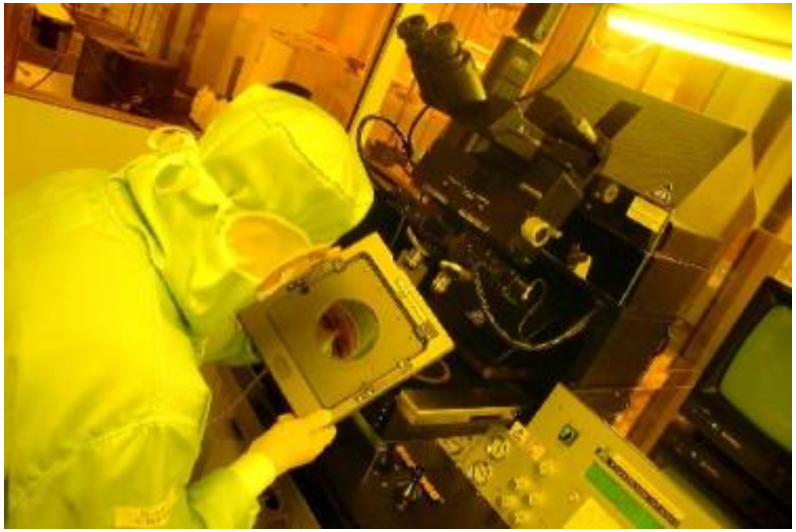


Materials:

- silicon substrate
- doped silicon
- polysilicon
- silicon oxide layers
- silicon nitride layers
- aluminum metal

Physical Electronics Laboratory
Andreas Hierlemann

Introduction - Cleanroom facilities

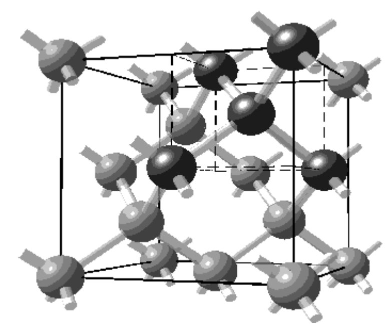


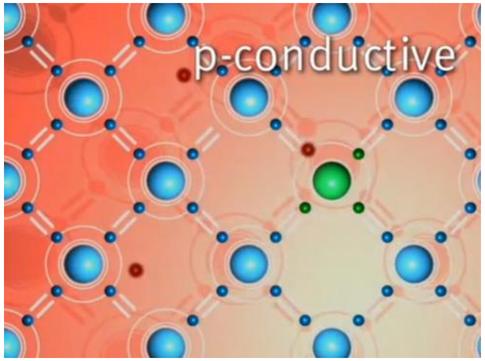
- **Dustfree Cleanrooms, Class:**
  - # of particles, in a cubic foot of air, > 0.5mm in size
  - typical hospital operating room: class 1000
  - outside air: class 500’000
  - circa 1980’s cleanrooms are class 100
  - most modern cleanrooms are class 1

- **Additional Requirements:**
  - temp. and humidity control
  - gas supply
  - waste management
  - safety equipment
  - clothing

Silicon bulk Material: Forms of Silicon

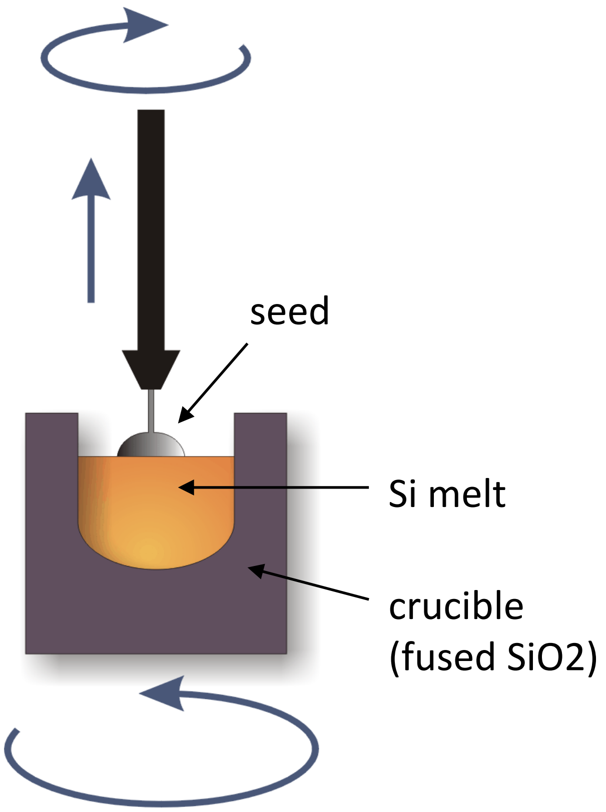
- naturally occurs in the form of silica (Quartz, sand, flint) and silicate rocks (SiO_2 combined with Al, Mn, Ca, Na, K, Fe,...)
- 2nd to oxygen in abundance (80 % of the Earth crust)
- is essential to the manufacture of glass
- early use in electronics: vacuum tubes (Silica), capacitors (Mica), resonators and filters (Quartz)





The Czochralski (CZ) method

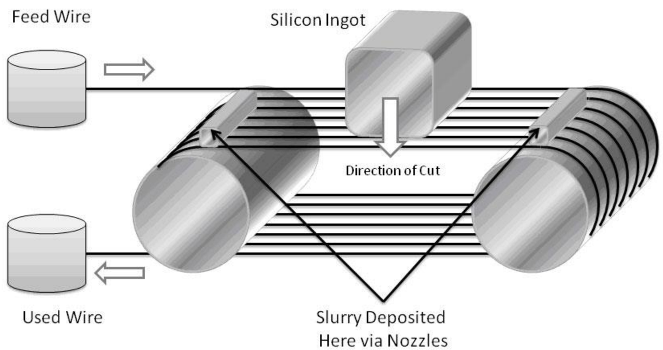
- > 80% of world production
- Si single crystal is grown from a crystal seed by pulling it from a molten and ultra-pure silicon melt (EGS)
- pull rate affects incorporation of impurities and influences the defect generation
- growth rate influences dopant distribution and the defect structure on a microscopic scale

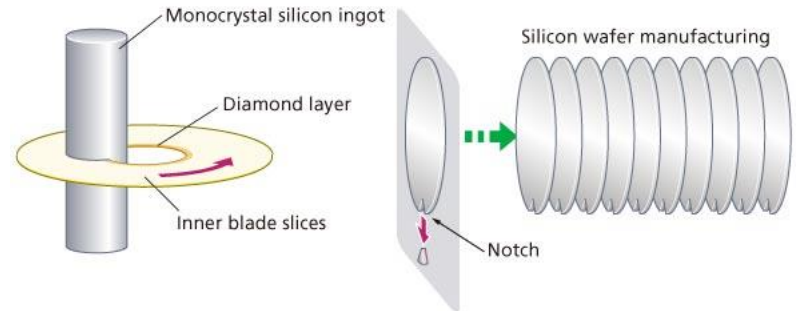


Czochralski growth: http://www.youtube.com/watch?v=xftnhfa-Dmo
Czochralski growth and impurity doping: http://www.youtube.com/watch?v=jh2z-g7GJxE

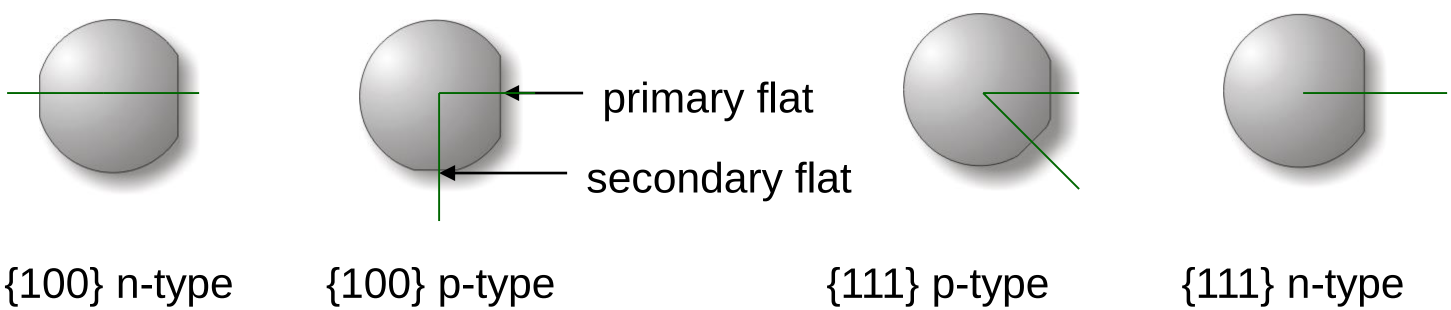
Silicon bulk Material: Cutting and Flat grinding

- Cutting the Silicon ingot into wafers

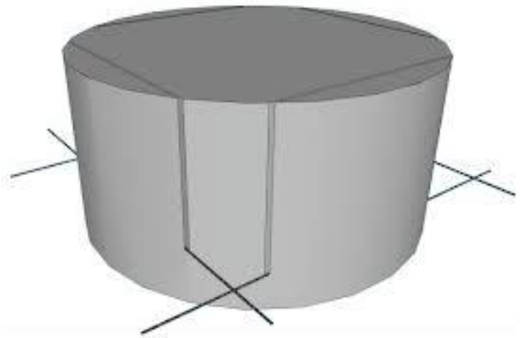




- Primary (orientation) and secondary (doping) flat grinding,
- crystal orientation is defined by x-ray technique, precision is +/- 1 um



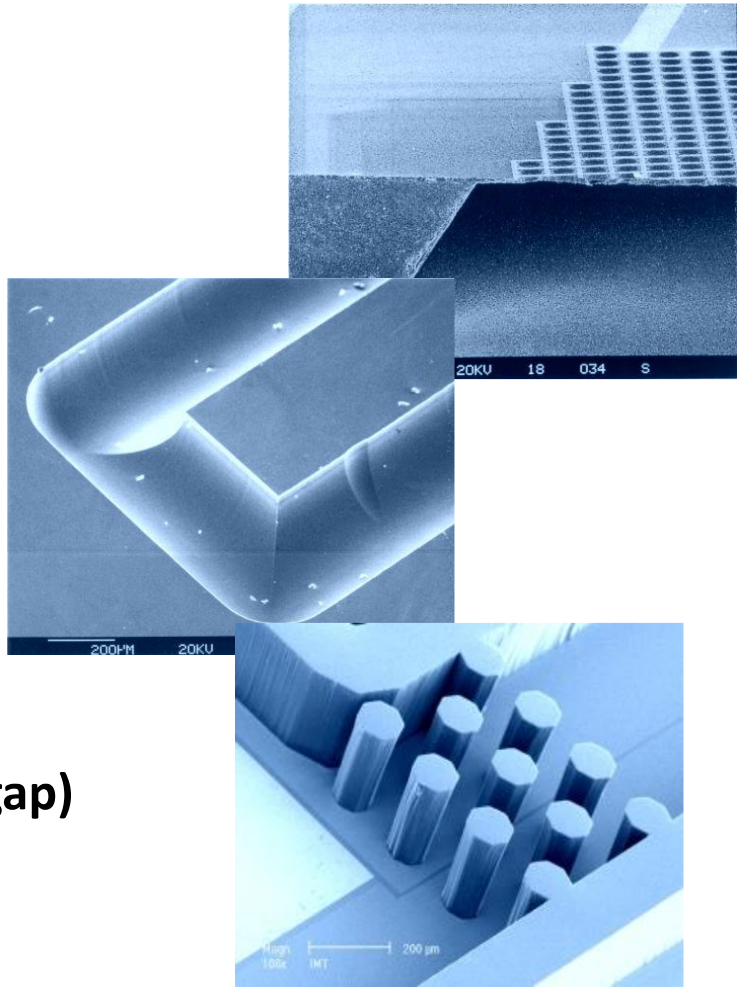
Silicon bulk Material: Pseudo square Silicon wafers for solar industry



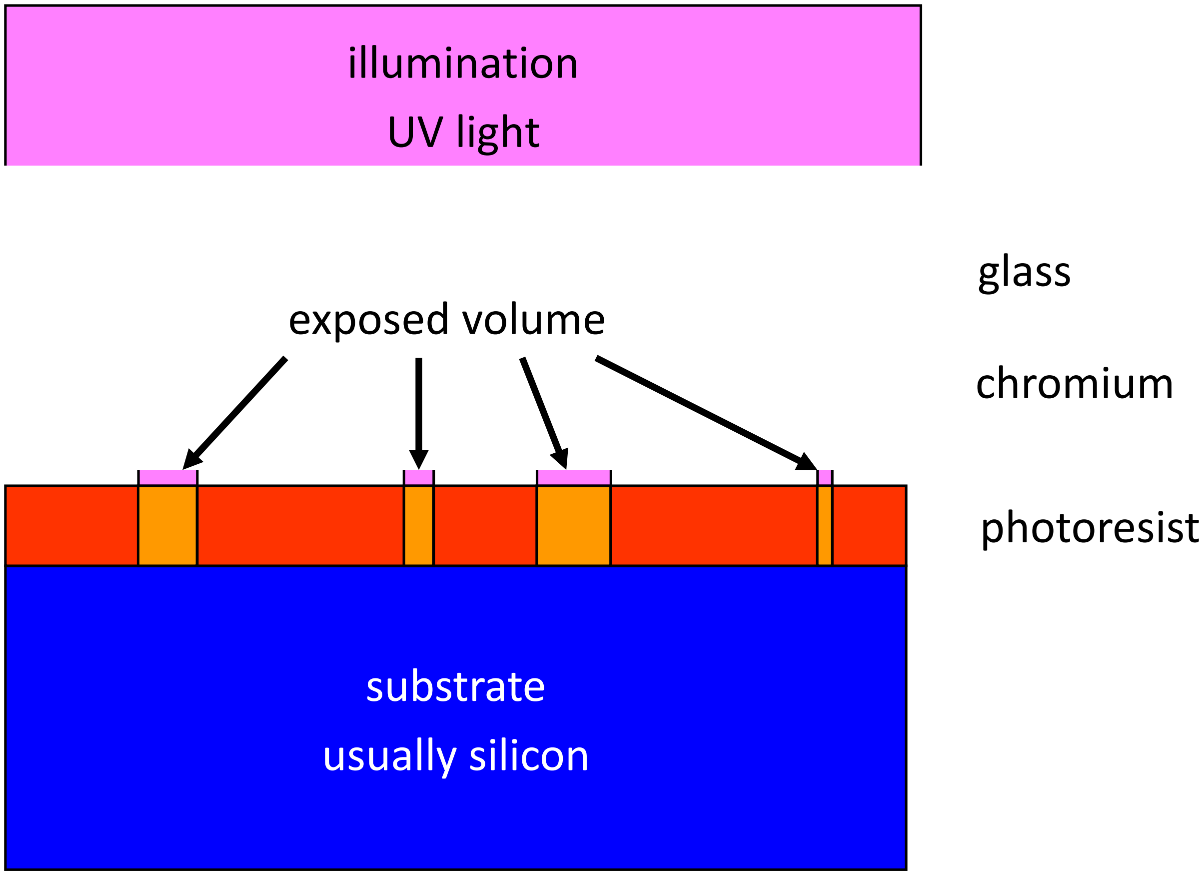
http://www.youtube.com/watch?v=-QPYw8EN4VM

Other Materials used for MEMS

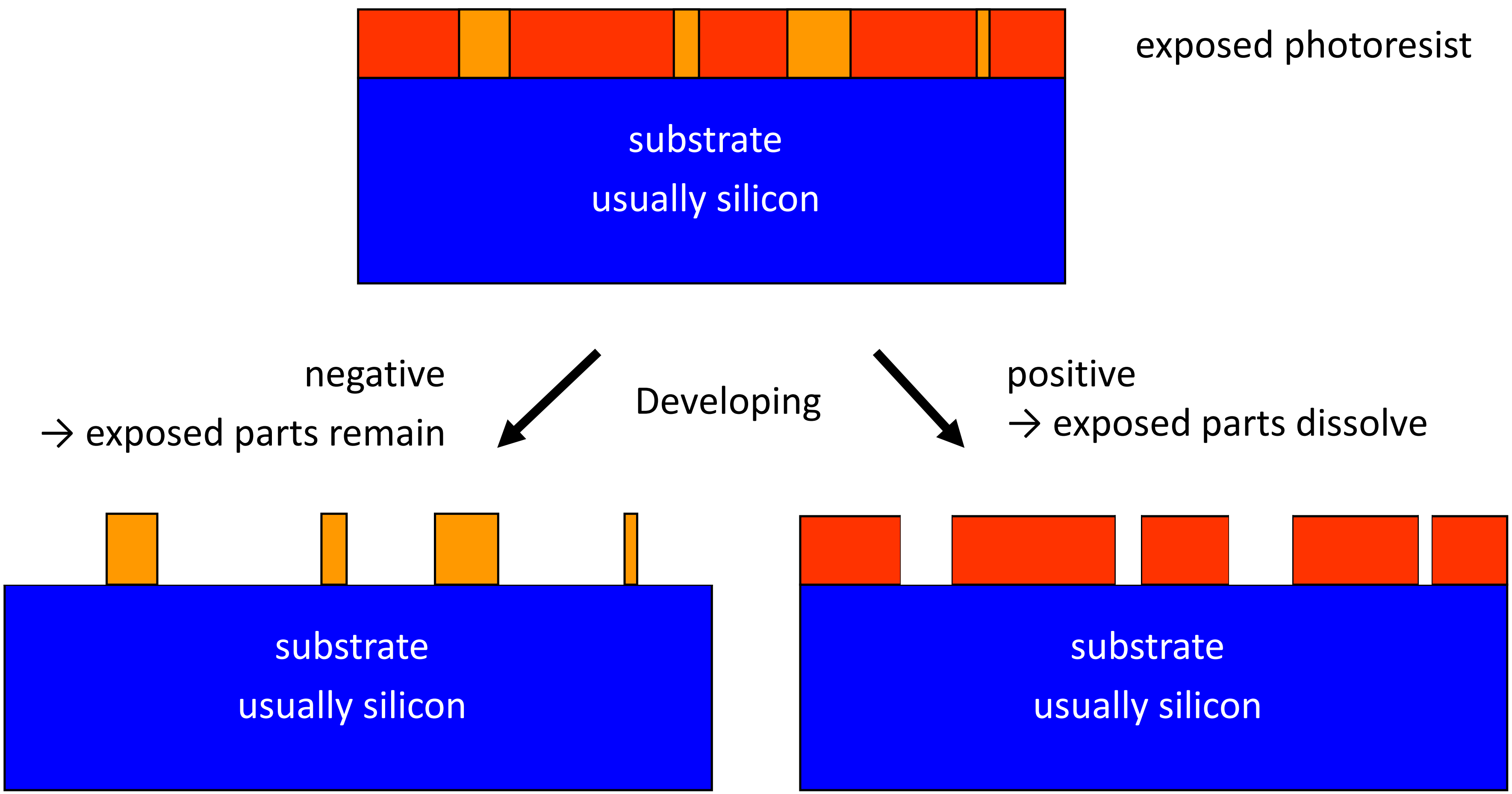
- **Silicon**
  - well established processes
    (bulk and surface micromachining)
  - mechanical, semiconductor properties
- **Glass**
  - well established processes
    (bulk micromachining and add-on layers)
  - optical, dielectric properties
- **Plastics**
  - good engineering know-how
  - low cost material
  - replication techniques
- **Ceramics (LTCC) + silicon carbide (high band gap)**
  - resistant to high temperature
  - mechanical, laser micromachining, molding



Pattern transfer by illumination of a mask into photoresist.

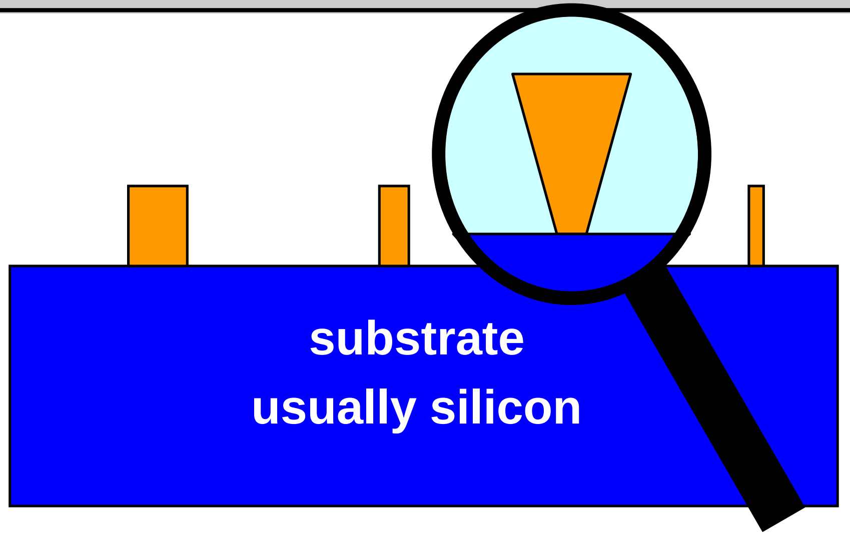


Lithography – Positive and negative Photoresist



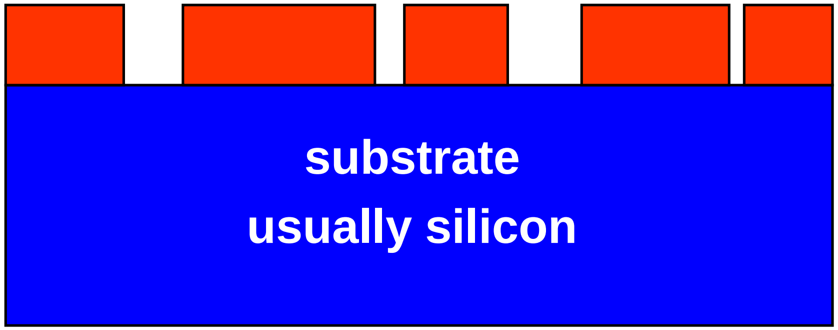
Lithography – negative Photoresist

- exposed resist remains
- excellent adhesion on silicon
- low contrast
- better for small exposed areas
- develloped mostly by organic solvents (swelling)
- overcut in side-walls
- very good for lift-off (metal leads)
- high chemical resistance
- very good for wet and dry etching (RIE)
- very senstive to humidity
- smallest feature size ca. 1.5 µm
- fair step coverage



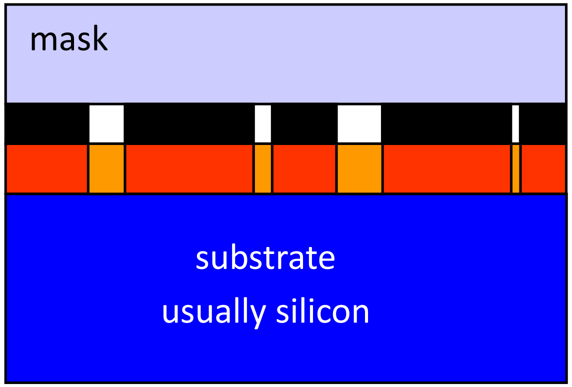
Lithography – positive Photoresist

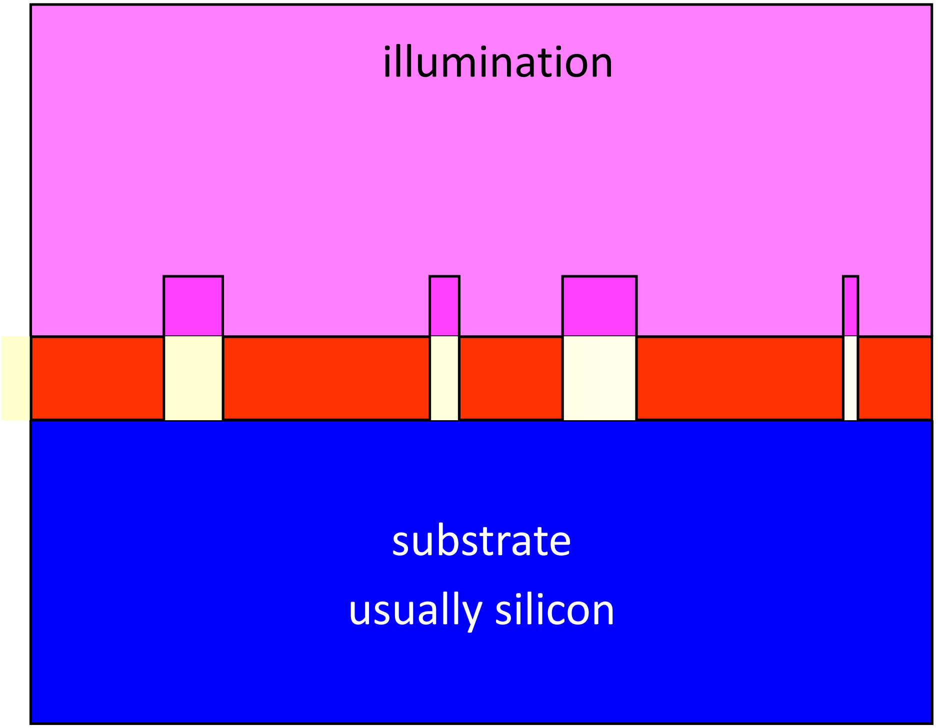
- unexposed resist reamains
- fair adhession on silicon (humidity)
- high contrast
- better for large exposed areas
- developed mostly by aqueous solutions
- almost vertical side-walls
- limited use for lift-off (metal lines/leads) (exception: e-beam lithography)
- fair resistance to wet and dry chemical etching
- removable with cheap solvents
- good step coverage



Lithography – contact exposure

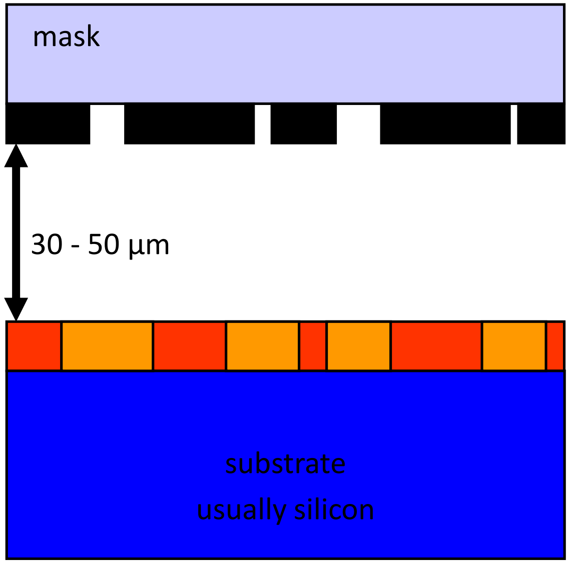
- 1:1 pattern transfer
- Wafer and mask in direct contact
- Very small patterns
- Very little diffraction on thin resist
- Mechanical damage to mask
- Mask cleaning
- Complete wafer is exposed

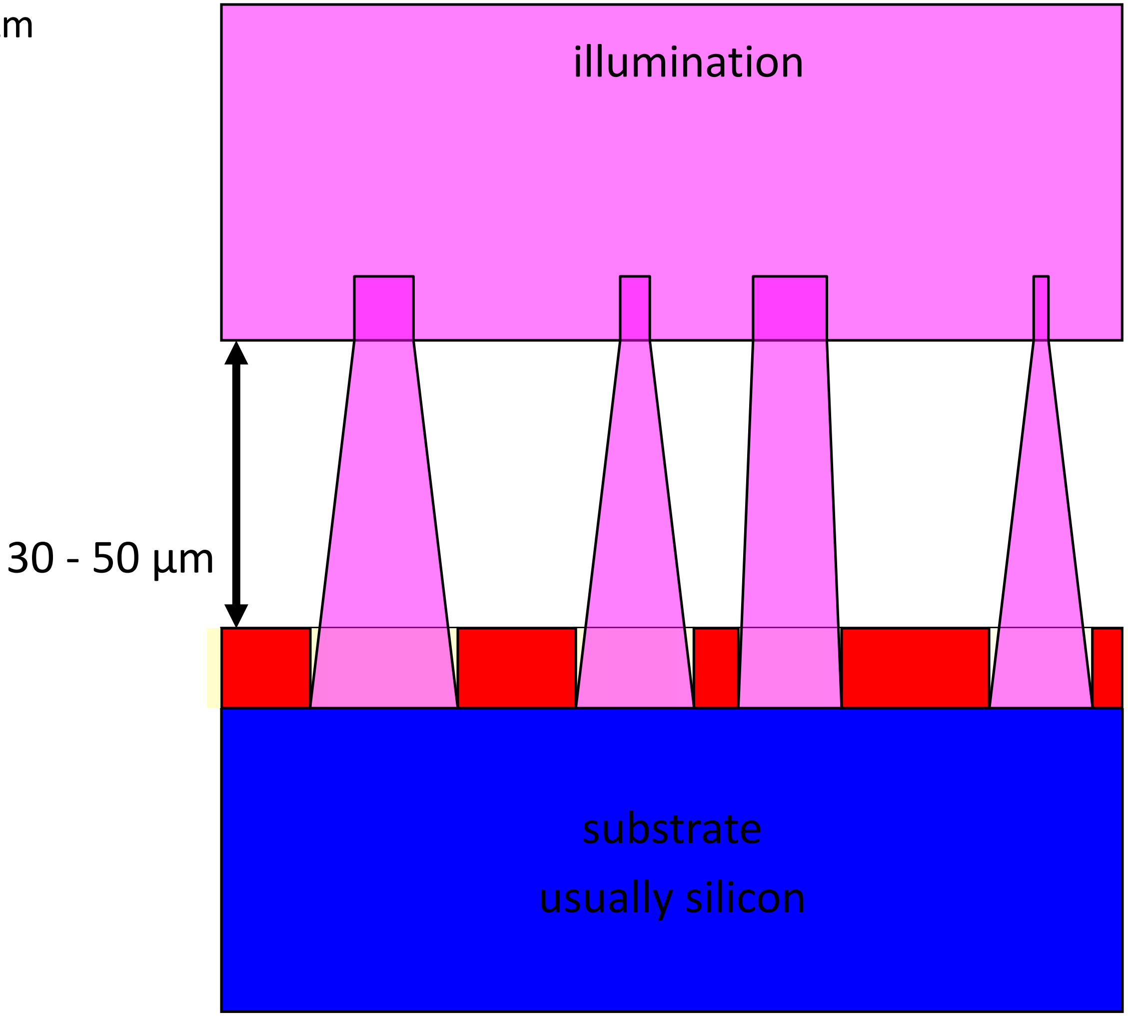




Lithography – proximity exposure

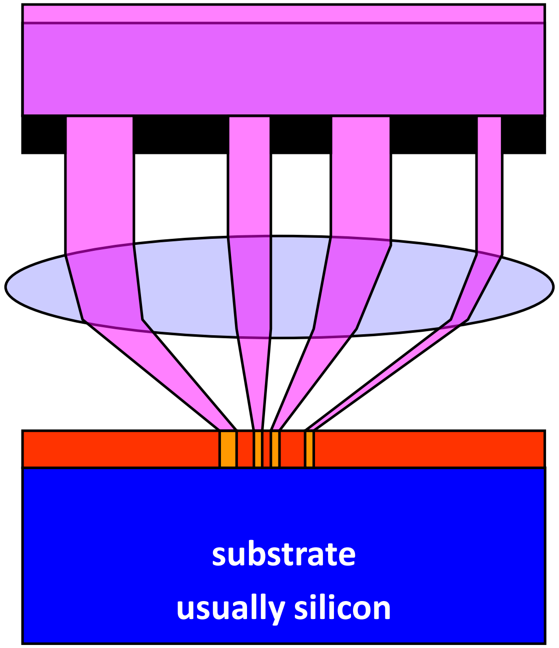
- Pattern worse than 1:1
- Wafer to mask distance about 50 µm
- Bent wafers or sensitive structures
- Large patterns
- Diffraction increases feature size
- No damage to mask
- No mask cleaning
- Complete wafer is exposed

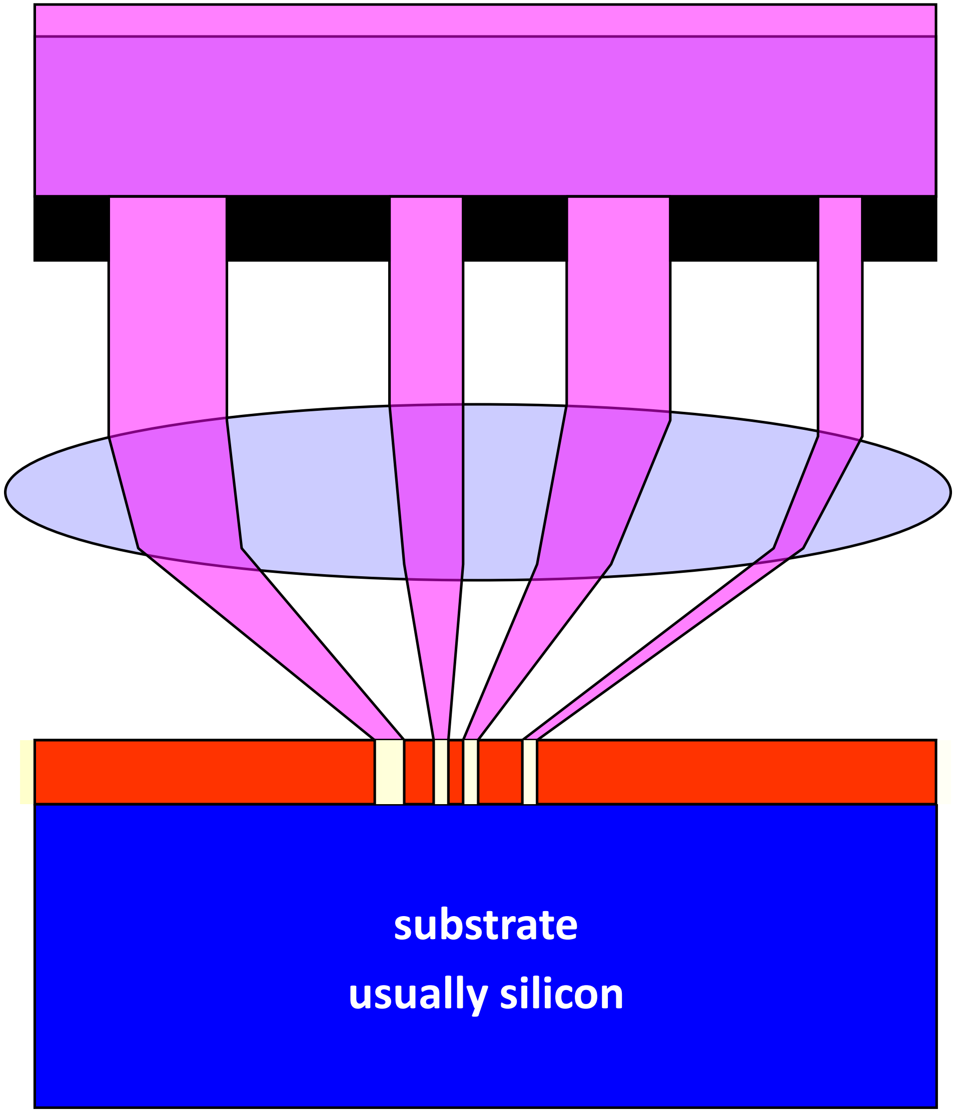




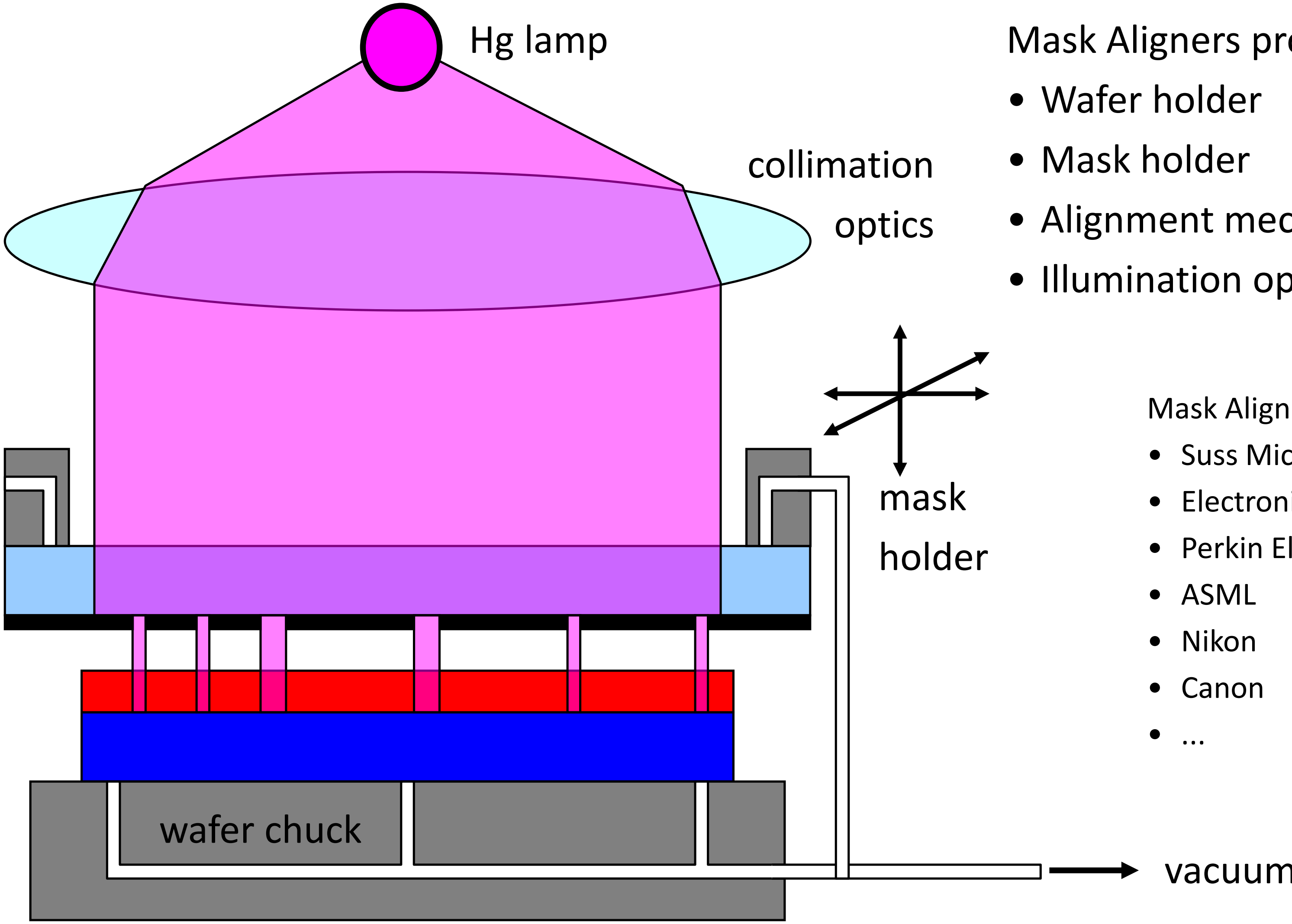
Lithography – projection exposure

- 1:n scaling, e.g. n=5
- Mask is optically projected onto wafer
- Extremly small patterns
- No mechanical damage to mask
- Very expensive
- Only part («die») of wafer is exposed





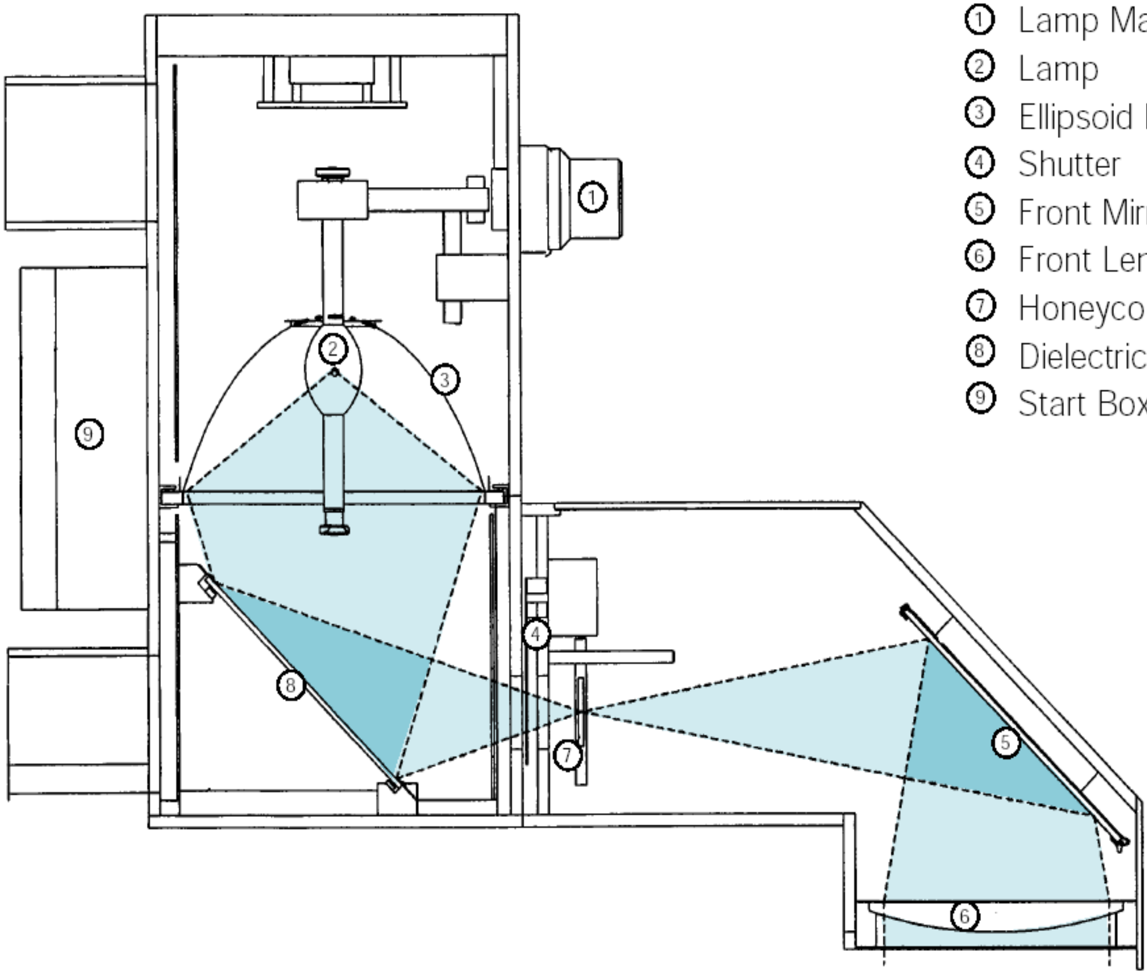
Lithography – Principle of Mask Aligners



Mask Aligners provide
- Wafer holder
- Mask holder
- Alignment mechanics
- Illumination optics

Mask Aligner Companies:
- Suss MicroTec
- Electronic Vision
- Perkin Elmer
- ASML
- Nikon
- Canon
- ...

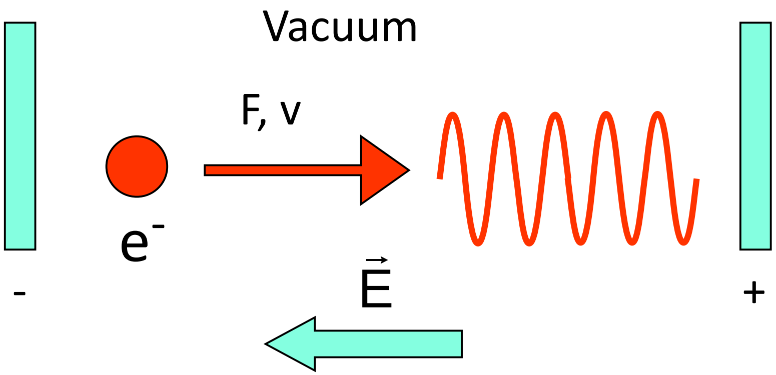
For example Karl Suss MA 1006



1. Lamp Manipulator
2. Lamp
3. Ellipsoid Mirror
4. Shutter
5. Front Mirror 45º
6. Front Lens
7. Honeycomp Condensor Lens
8. Dielectrical Mirror 45º
9. Start Box

E-Beam Lithography

Electrons interact with electric and magnetic fields

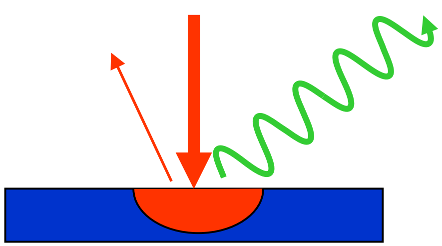


$$\lambda = \frac{h}{p}; \qquad E = \frac{m}{2}v^2 = eU$$

$$\Rightarrow \lambda = \frac{h}{\sqrt{2 m_{electron} eU}}$$

$$\left.\begin{aligned} h &= 6.62 \times 10^{-34}\ \text{Js} \\ m &= 9.11 \times 10^{-31}\ \text{kg} \\ e &= 1.60 \times 10^{-19}\ \text{C} \end{aligned}\right\} \Rightarrow \lambda \approx 1.23\ \text{nm}/\sqrt{\text{V}}$$

Electrons strongly interact with matter

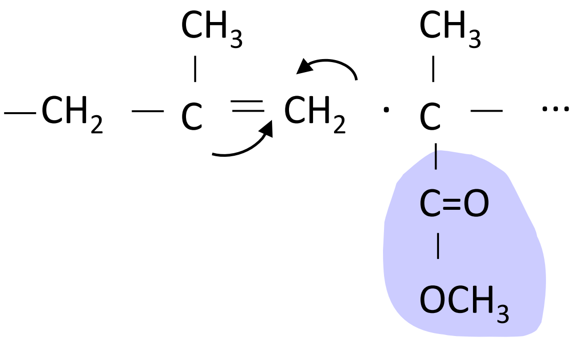


The penetration depth of electrons is small,
it depends on its energy and the substrate!
The kinetic energy of the electron is released into secondary particles and heat

E-beam Lithography

thermal effect: Electron-beam evaporator for thin film technology

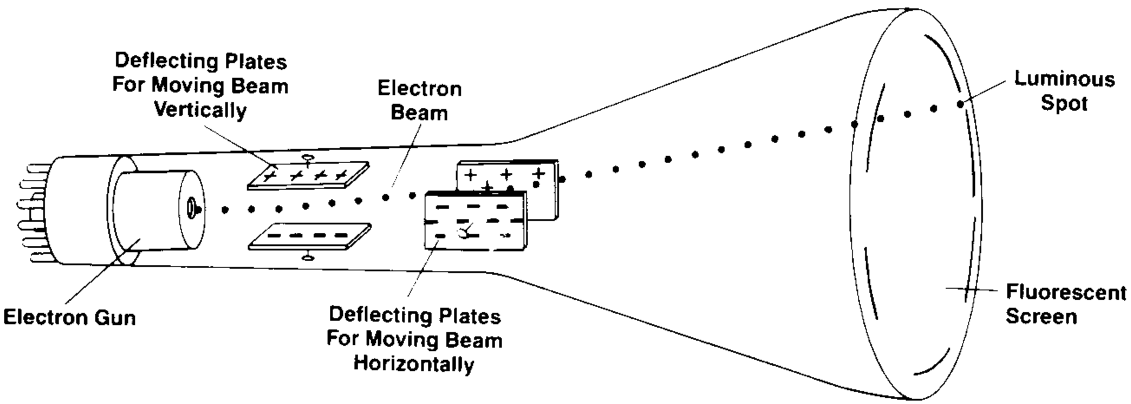
Poly (methylmethacrylat)



ester side chain

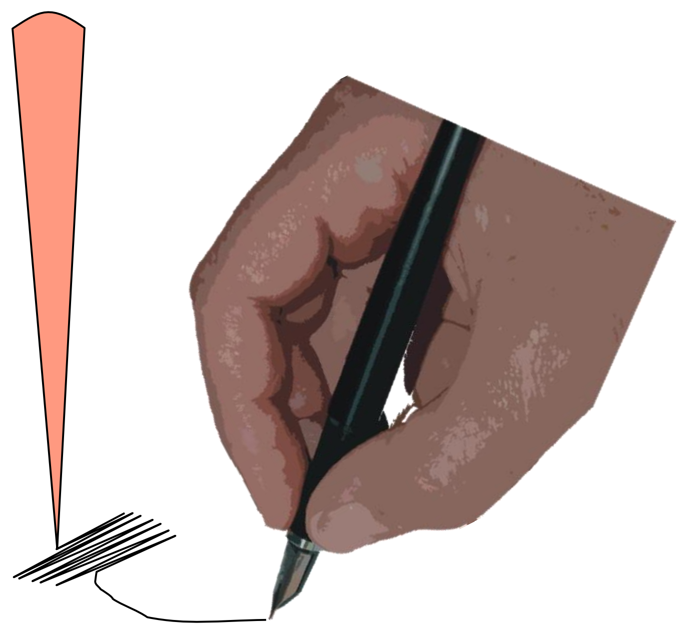
chemical effect: Bond breaking stops by (re)combination of two unzipped pieces

E-beam Lithography



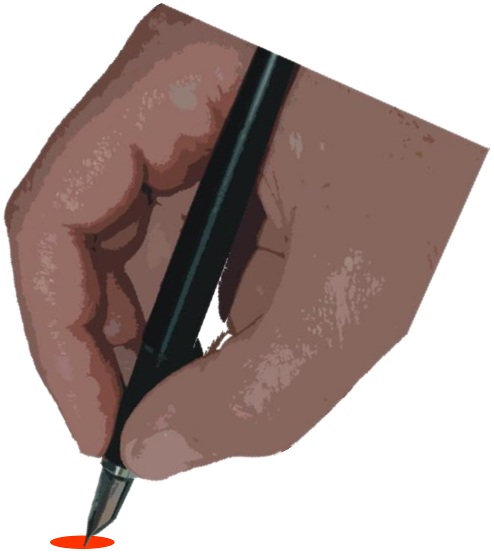
A ray of electrons, a "pencil", can be deflected by transverse electric fields (c.f. CRT!).

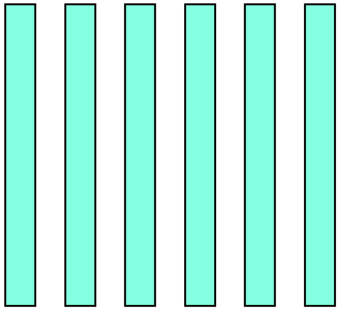
$\Rightarrow$ electron beam writing!



E-beam Lithography - Resolution

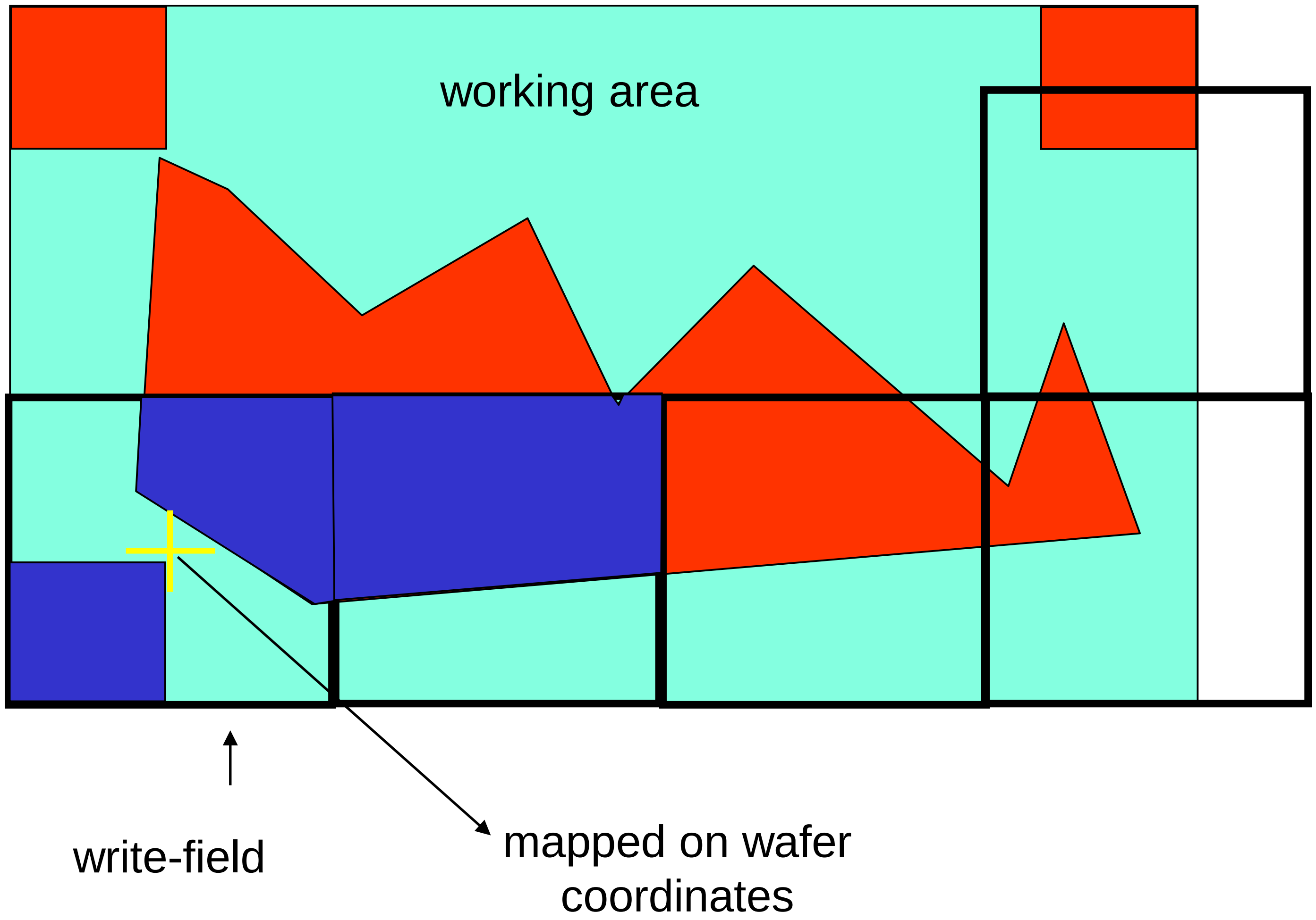
feature size = f (beam diameter, interaction, interaction time, development)



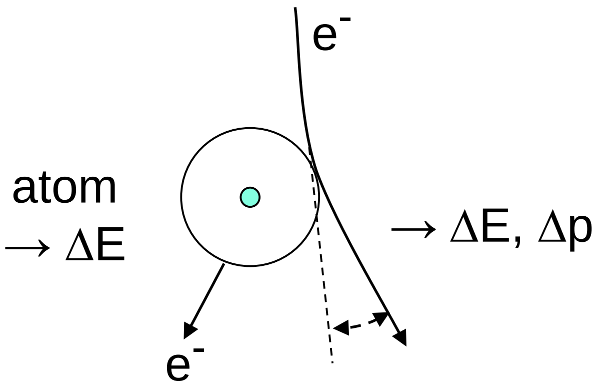


$\Rightarrow$ Equal lines and spaces is the only sensible way to characterize resolution of EBL

Concepts of writing - write field stitching

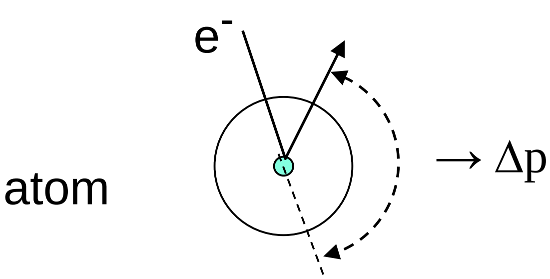


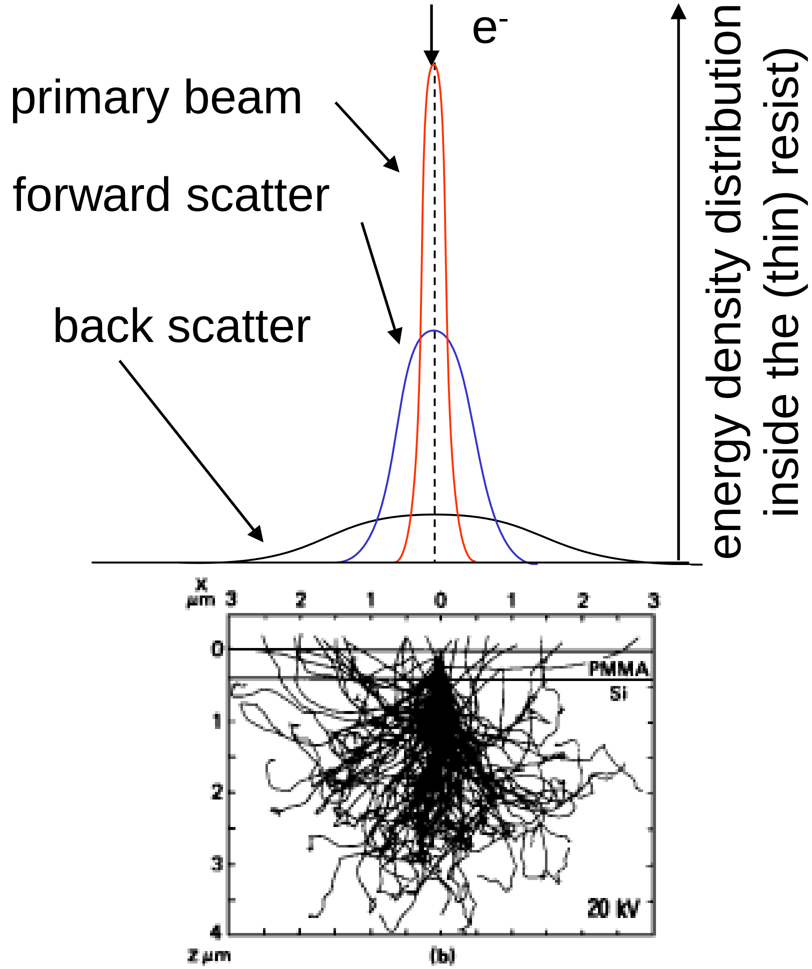
forward scattering (inelastic)



“secondary electron”

back scattering (elastic)

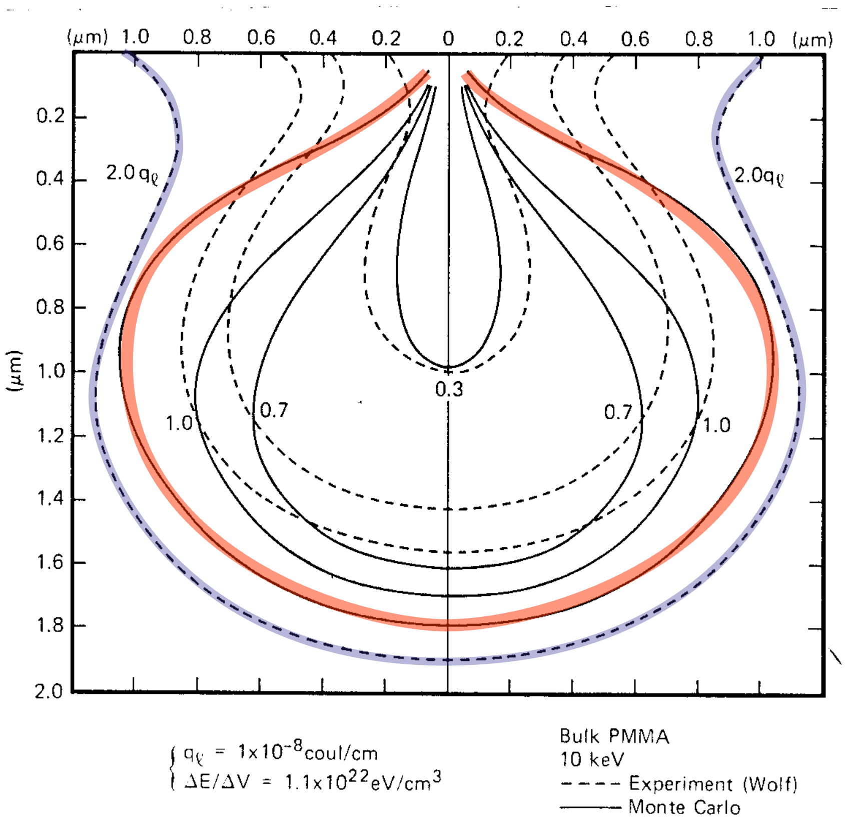




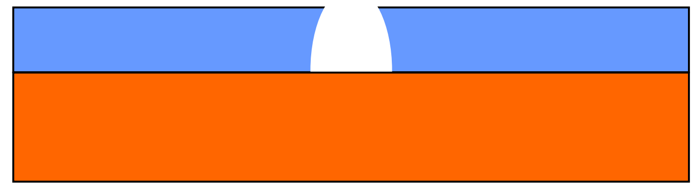
D.F. Kyser, N.S. Viswanathan, JVST **12,** 1305 (1975)

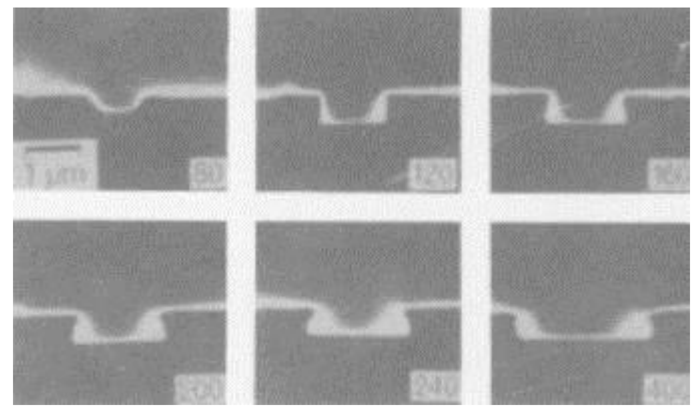
Electron - resist interaction

contours of iso-dose
lines in the resist



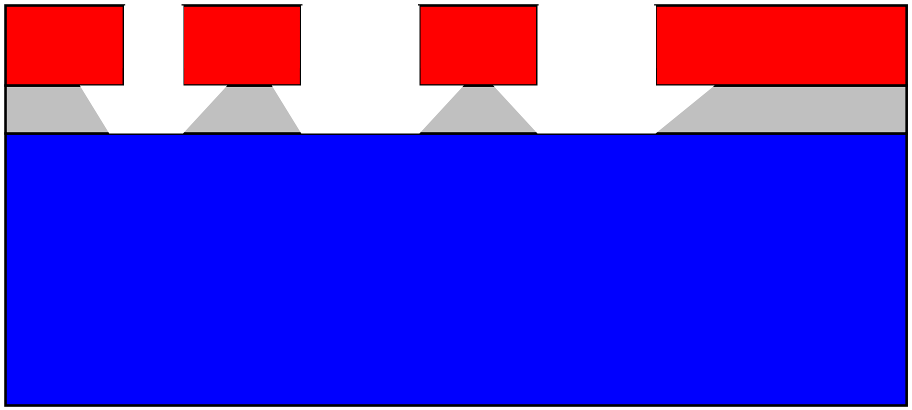
contours of iso-dose
lines in the resist





resist profile as function of dose:
80, 120, 160, and
200, 240, 400 μC/cm^2

1) Isotropic Etching

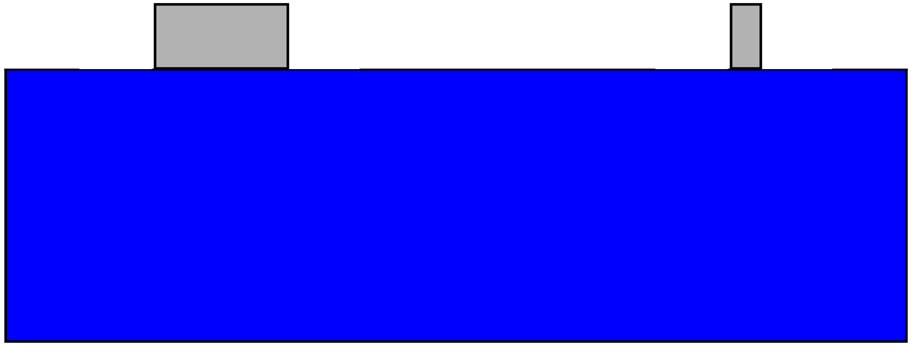


patterned photoresist

metal coating

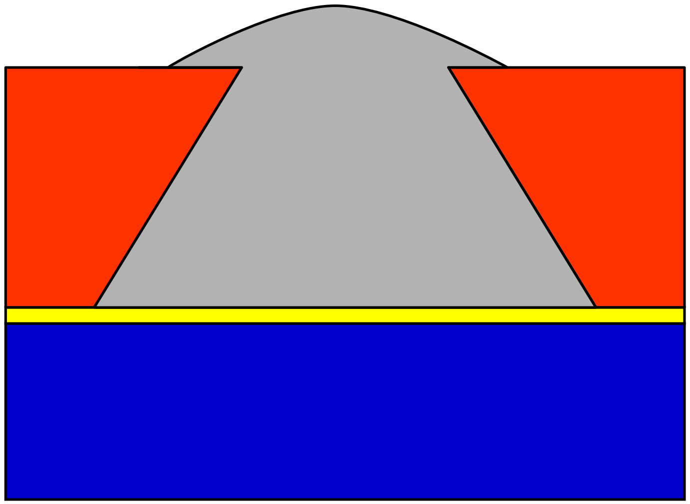
substrate

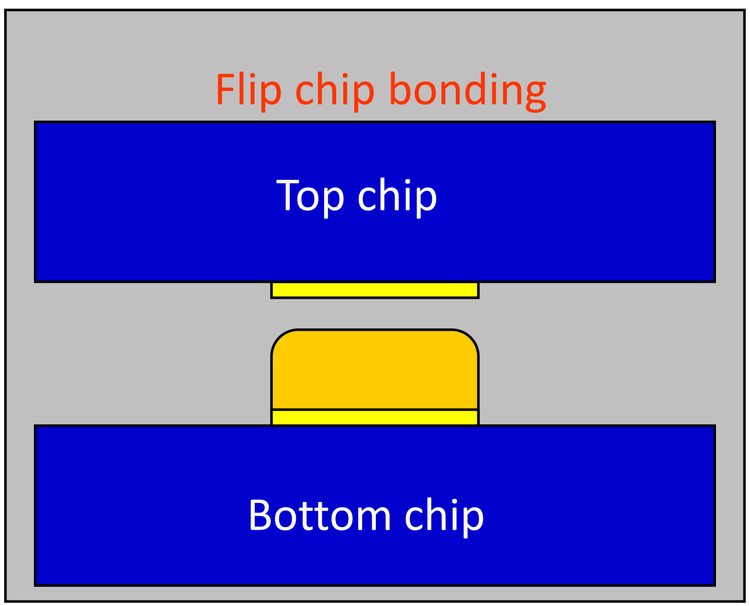
2) Lift-Off



1. patterned photoresist with undercut
2. de-scum
3. metal evaporation

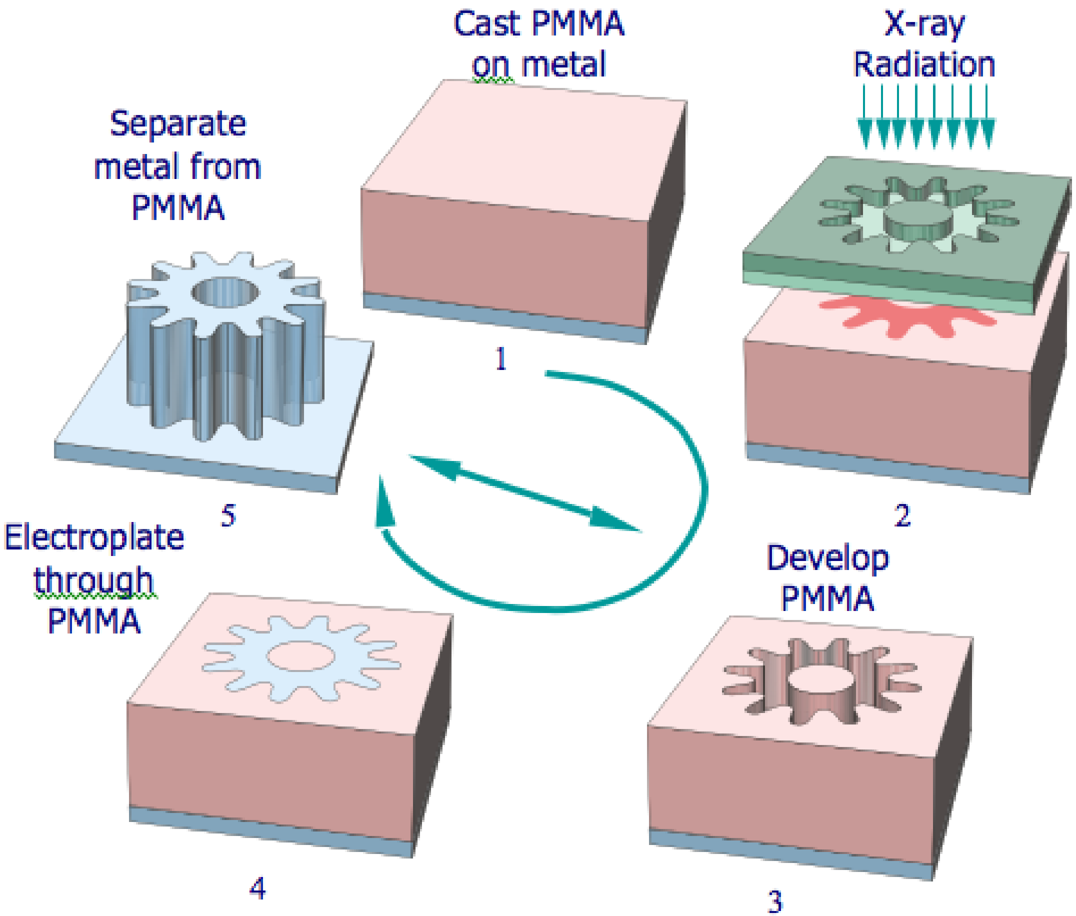
Pattern transfer – eletroplating with thick resist

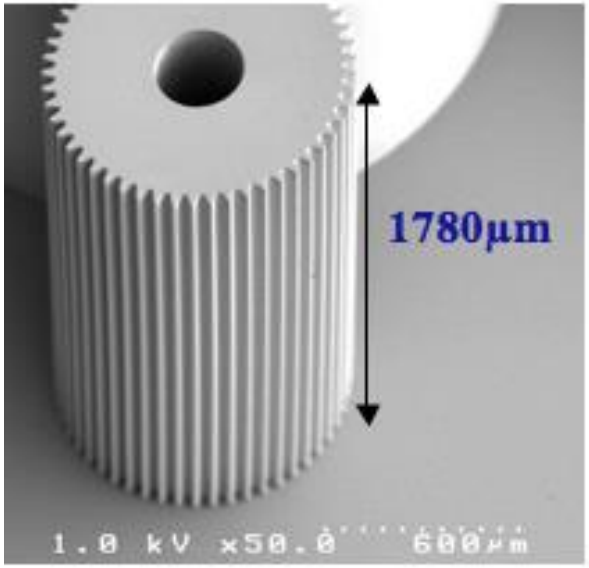


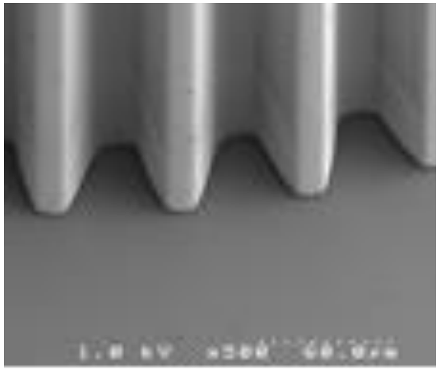


1. Thick resist as lateral limits for electroplating (galvanic growth)
2. Starting metal layer
3. Aqueous solution with metal ions
4. By aplying a voltage to the substrate, metal ion are reduced on starting metal layer
5. Resist is removed
6. Substrate can be removed as well
7. Small metal parts with very high precision or solder bumps for flip chip bonding

Pattern transfer – LIGA

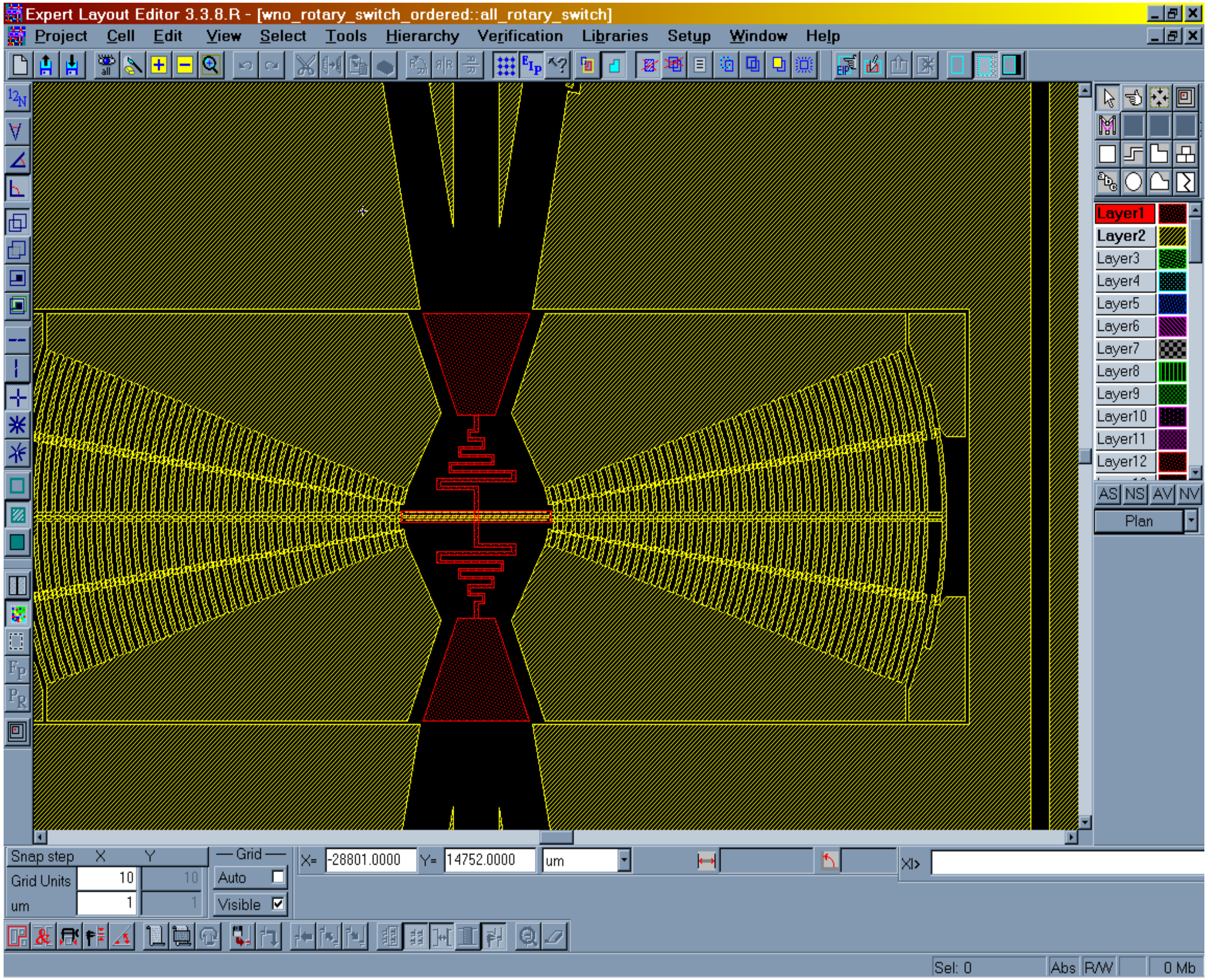




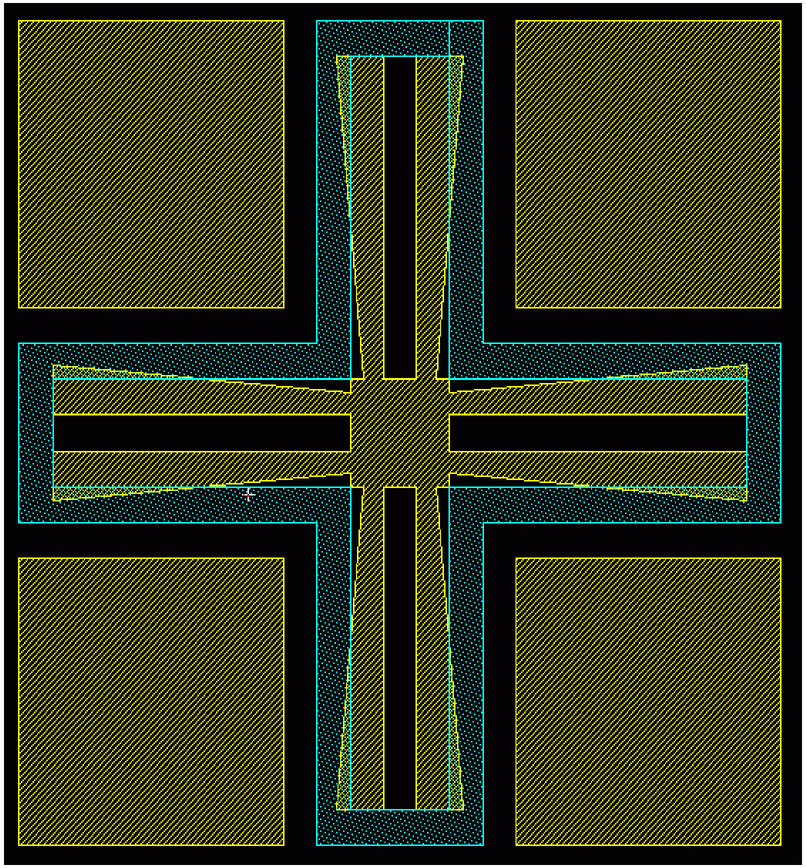


Source: MEMS Exchange.org

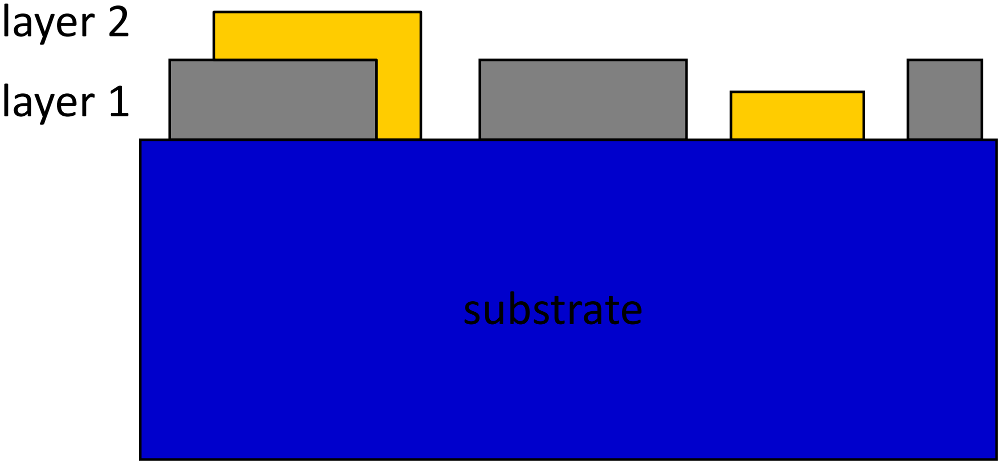
Pattern transfer – Mask design – layout editor



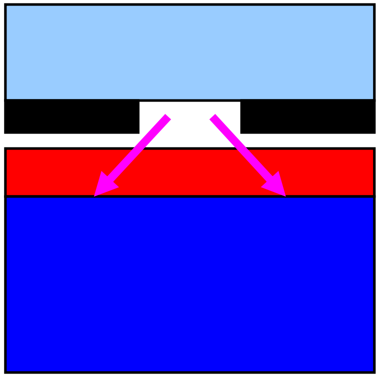
Pattern transfer – Mask design – alignment



- Multiple alignments of masks
- Precise alignment of patterns
- Standard mask aligner 1- 2µm
  - sufficient for MEMS
- Stepper with image recognition:
  - less than 100nm
  - necessary for micro-electronics

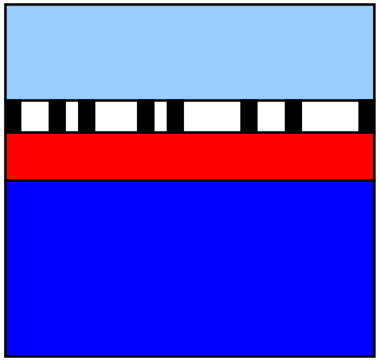


- **Resolution limit**:
  - wavelength/2 ≈ 200 nm
  - Diffraction due to distance = thickness of photoresist



Photolithography:

  - near field holography



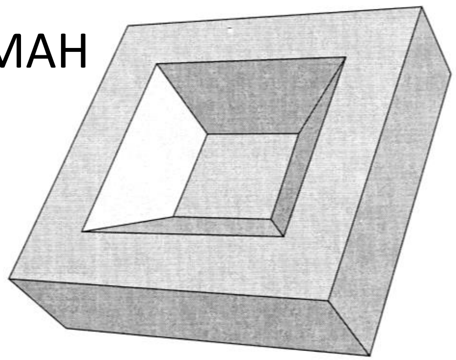
- **E-beam**
  - High resolution, not diffraction limited
  - PMMA (not sensitive to visible light)
  - proximity correction
- **X-Ray/Synchroton radiation**
  - expensive
  - in reflection
- **X-UV**
  - optics are a problem

Bulk vs surface Micromachining

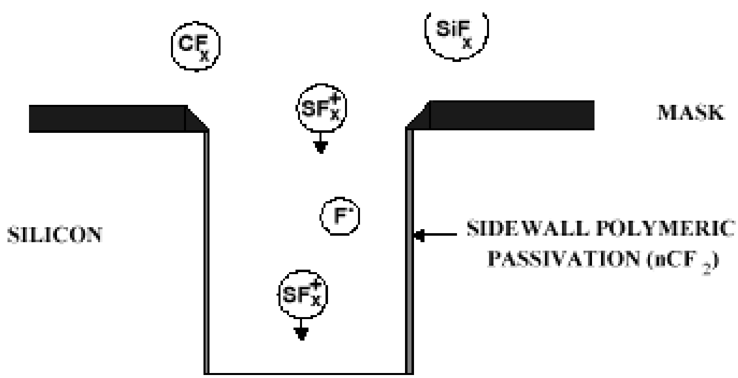
- **Bulk micromachining**

  Anisotropic etching

Wet: KOH, TMAH

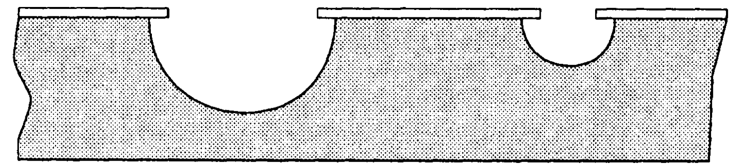


Dry: D



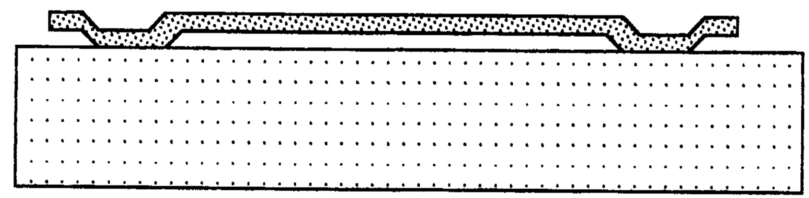
- **Bulk micromachining**

  Isotropic etching (wet or dry)



- **Surface micromachining**

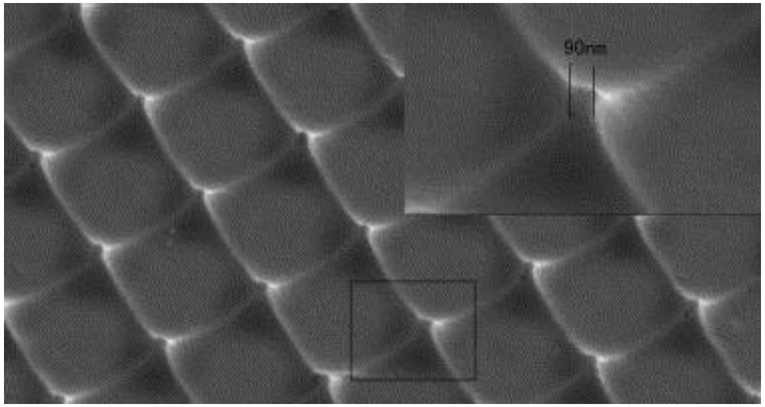
  Wet or dry etching



From G.T.A. Kovacs, Micromachined Transducers Sourcebook, 1998 M. Madou, Fundamentals of Microfabrication, 1997

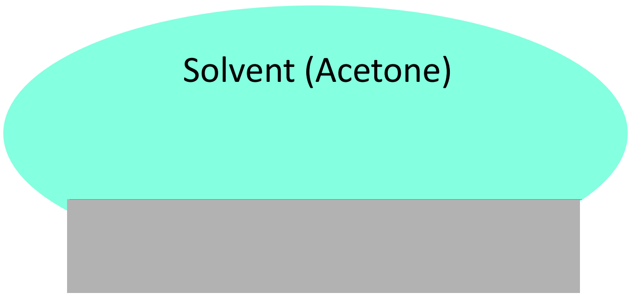
Bulk Micromachining – Wet Etching

- Etch rate
  Rate of material removal (µm/min)
  Function of concentration, mixing, temperature, …
  wide range
- Etch selectivity
  Relative (ratio) of the etch rate of the film to the mask, substrate, or another film.
  Trade off between etch rate and selectivity
- Etch geometry
  sidewall slope (degree of anisotropy)
- Etchants
  Mixtures of acids, bases, and water: HF, HPO_3, H_2SO_4, KOH, HCL,
  Solubility limit: 10:1, 5:1
- Materials
  Si, SiO_2, Si_3N_4, PR, Al, Au, Cu, …



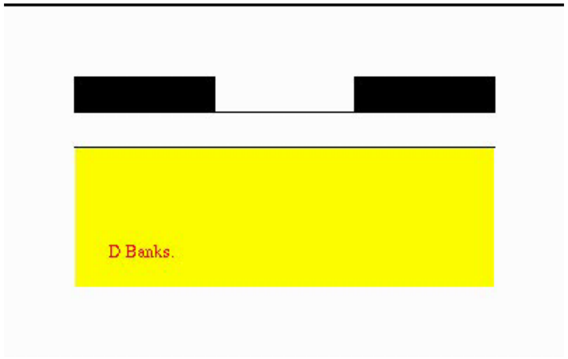
Bulk Micromachining – Wet Etching

- **Dissolution process:**
  Dissolution of the material in a liquid solvent without any change of the chemical nature of the dissolved species



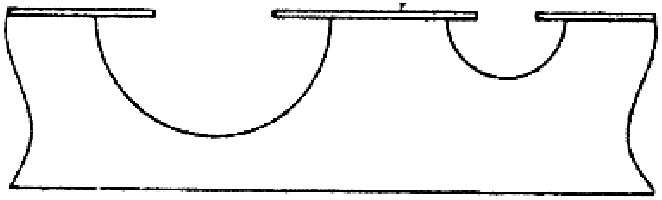
- **Oxidation -reduction process followed by dissolution:**
  conversion of the material being etched to soluble higher oxidation state

- **Factors affecting etching reactions**
  - Activation limited process: limitation by the chemical reactivity of the species involved in a sequential step of the total reaction
  - Diffusion limited process: limitation by the speed at which fresh reactant can be supplied to the surface

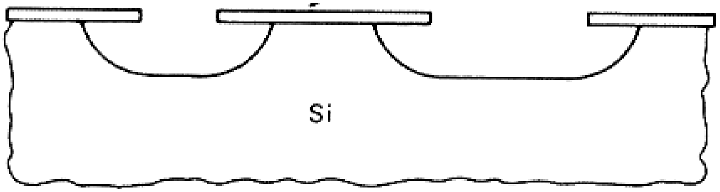


Agitation effect:

With agitation, the features approaches an ideal round cup



Without agitation, no fresh reactant can be supplied to the surface



Isotropic Wet Etching - Silicon in HNA

- HNA: Hydrofluoric acid (HF)
  Nitric acid (HNO_3)
  Acetic acid (Ch_3COOH)

$$18\ HF + 4HNO_3 + 3Si \Rightarrow 3H_2SiF_6 + 4NO + 8H_2O$$

  - HNO_3 drives oxidation of silicon to form SiO_2
  - HF attacks SiO_2 to form H_2SiF_6
  - CH3COOH prevents dissociation of HNO_3 into NO_3^- or NO_2^-

- Mainly used for cleaning, shaping and polishing compositional features
- Rounding of sharp anisotropically etched corners to avoid stress concentration
- Removing of roughness after dry or anisotropic etching

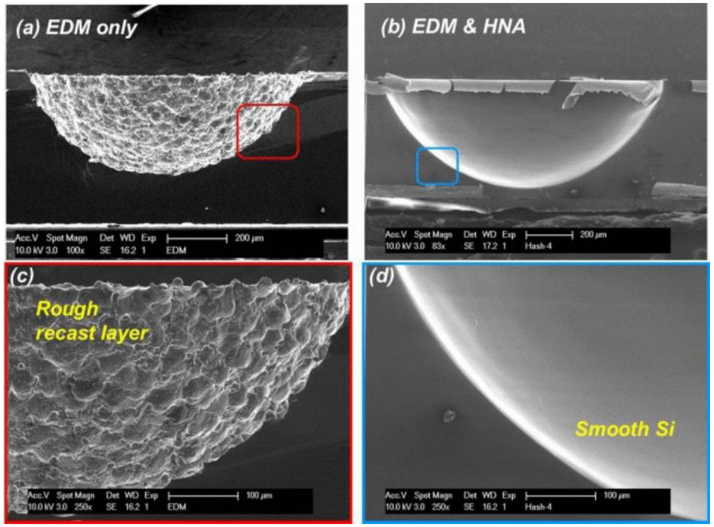


Illustration from 2012 IEEE 25th International Conference on, Issue Date: Jan. 29 2012-Feb. 2 2012, Written by: Chan, M.L.; Fonda, P.; Reyes, C.; Xie, J.; Najar, H.; Lin, L.; Yamazaki, K.; Horsley, D.A.

Isotropic Wet Etching – insulators and dielectrics

- **General etching properties of insulators and dielectrics**
  - Amorphous or micro-crystalline => classified as glasses
  - Chemically relatively inert =>highly reactive media for etching.

- **Single oxide example: SIO_2**
  - Etchants for SIO_2 are almost exclusively based on aqueous fluoride solutions, usually HF. With the addition of a buffer (NH_4F), the pH can be controlled and the solution is then called BHF.
  - BHF is important in pattern etching of SIO_2 films using photoresist masks where attack of the photoresist masking layer must be minimized

- **binary oxide example: Borosilicate (BSG,Pyrex)**
  - Important as dopant source, and silicon passivation and planarization
  - PECVD polysilicon is used as etch mask in HF 50%

Isotropic Wet Etching – insulators and dielectrics

SiO2 etch by hydrofluoric Acid (BHF)

Selective (room temperature)

- etches SiO_2 and not Si
- will also attack Al, Si_2N_4, …

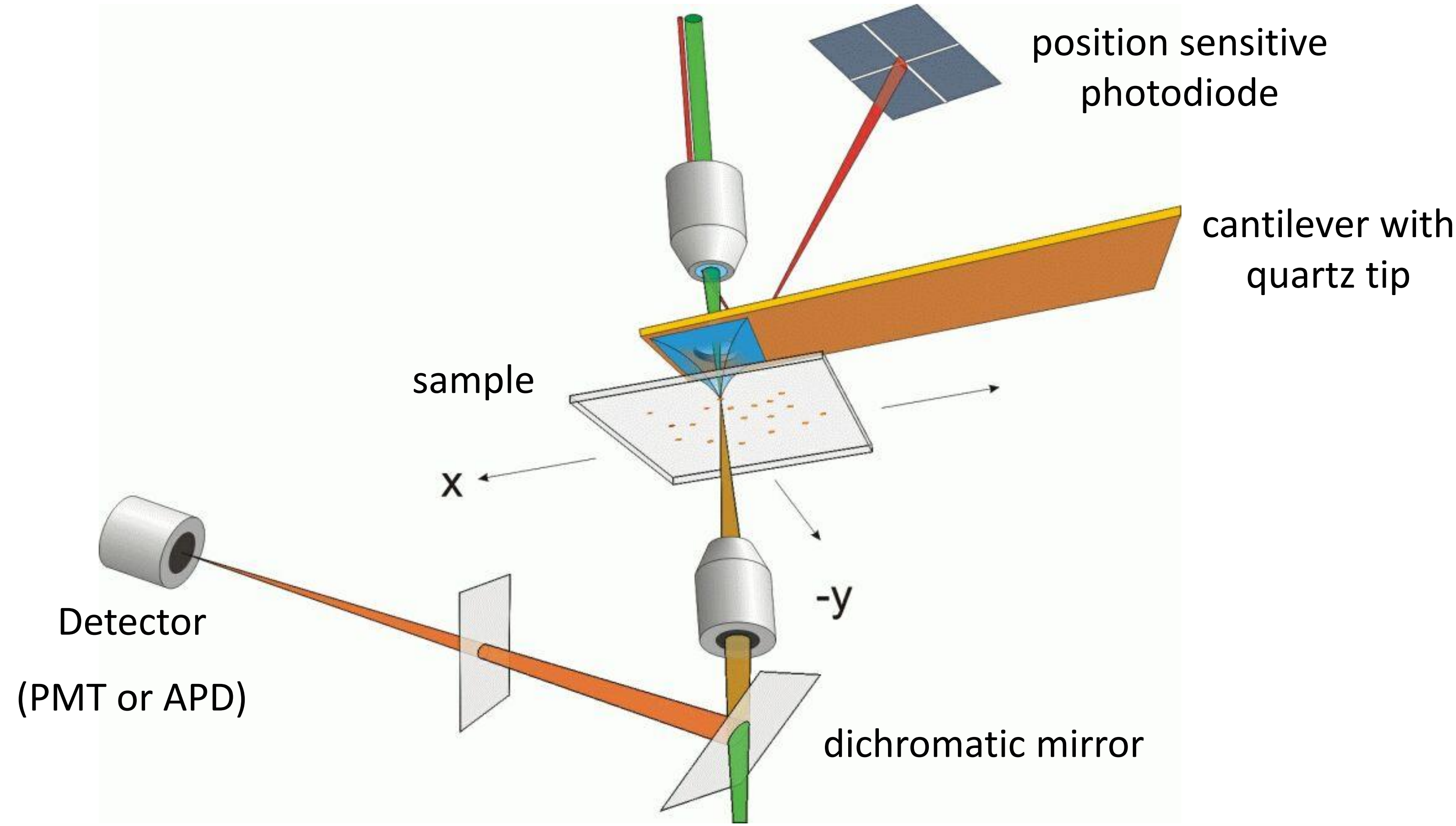
Rate depends strongly on concentration

- maximum: 49% HF ("concentrated") ~ >2 µm/min
- controlled: 5 to 50:1 ("timed") ~ <0.1 µm/min

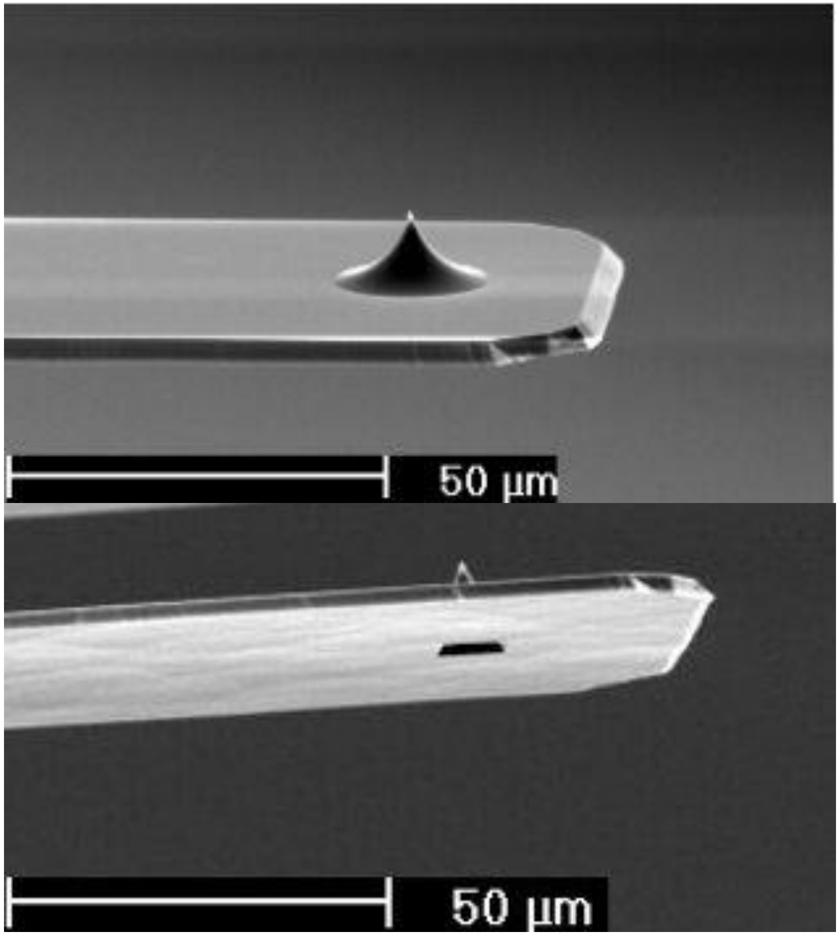
Dangerous!

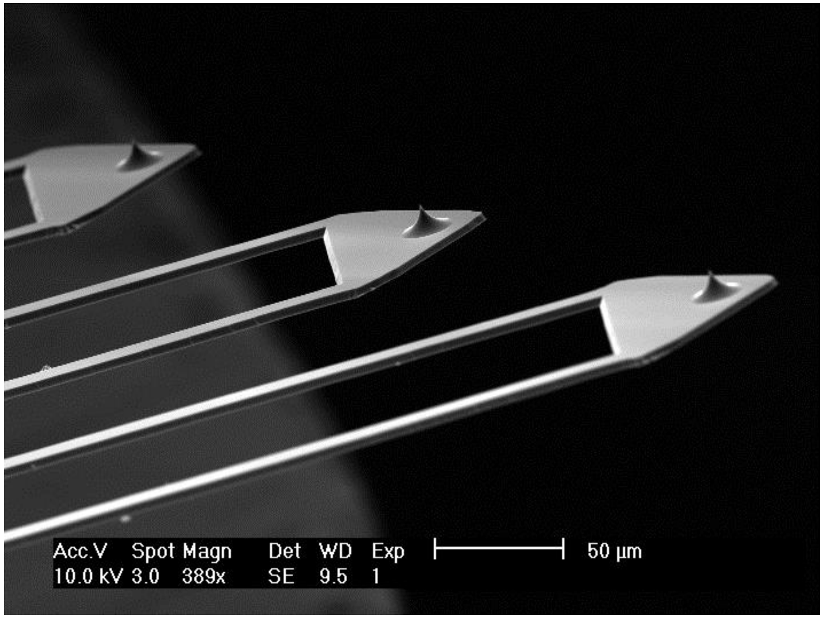
- not a strong acid
- deceptive (looks just like water)
- penetrates skin (adsorption) and attacks slowly
- will target bones (salve is made of calcium)

Isotropic Applications: SNOM quartz tips

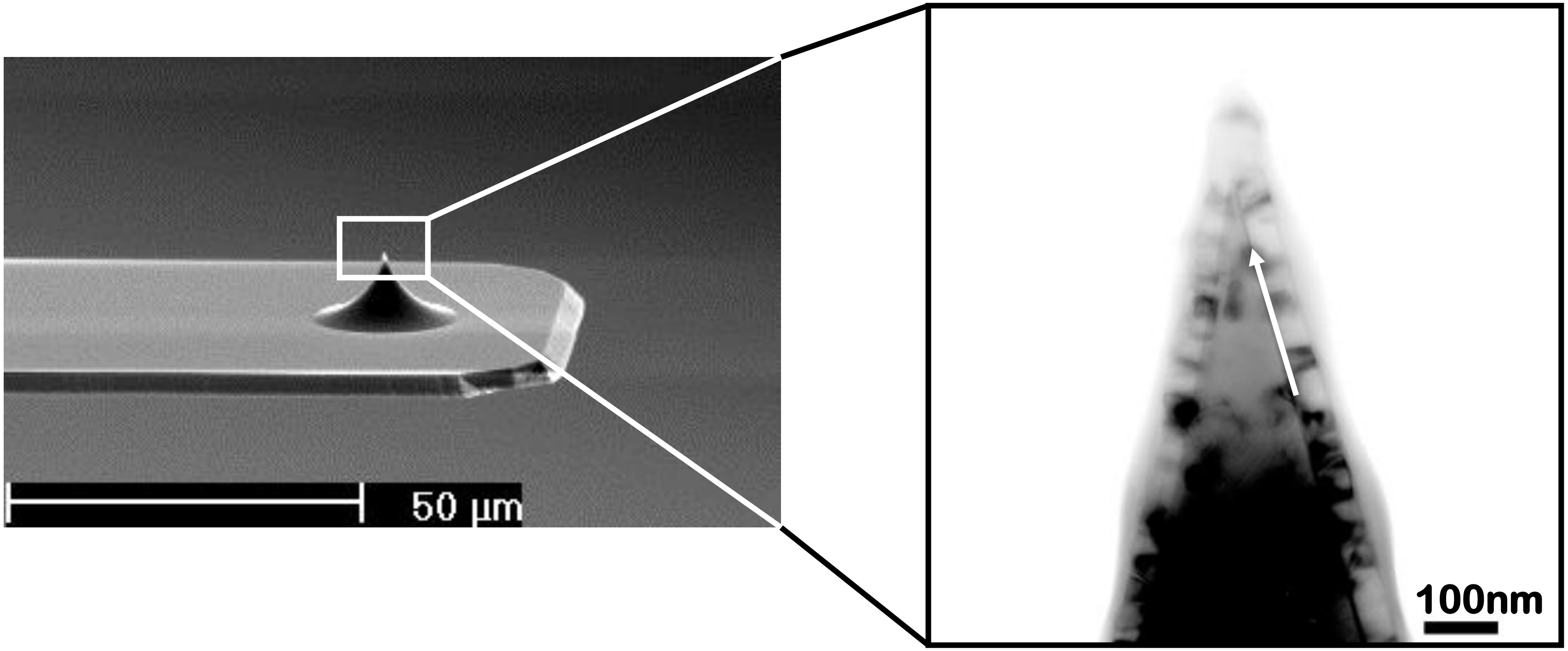


Isotropic Applications: SNOM quartz tips

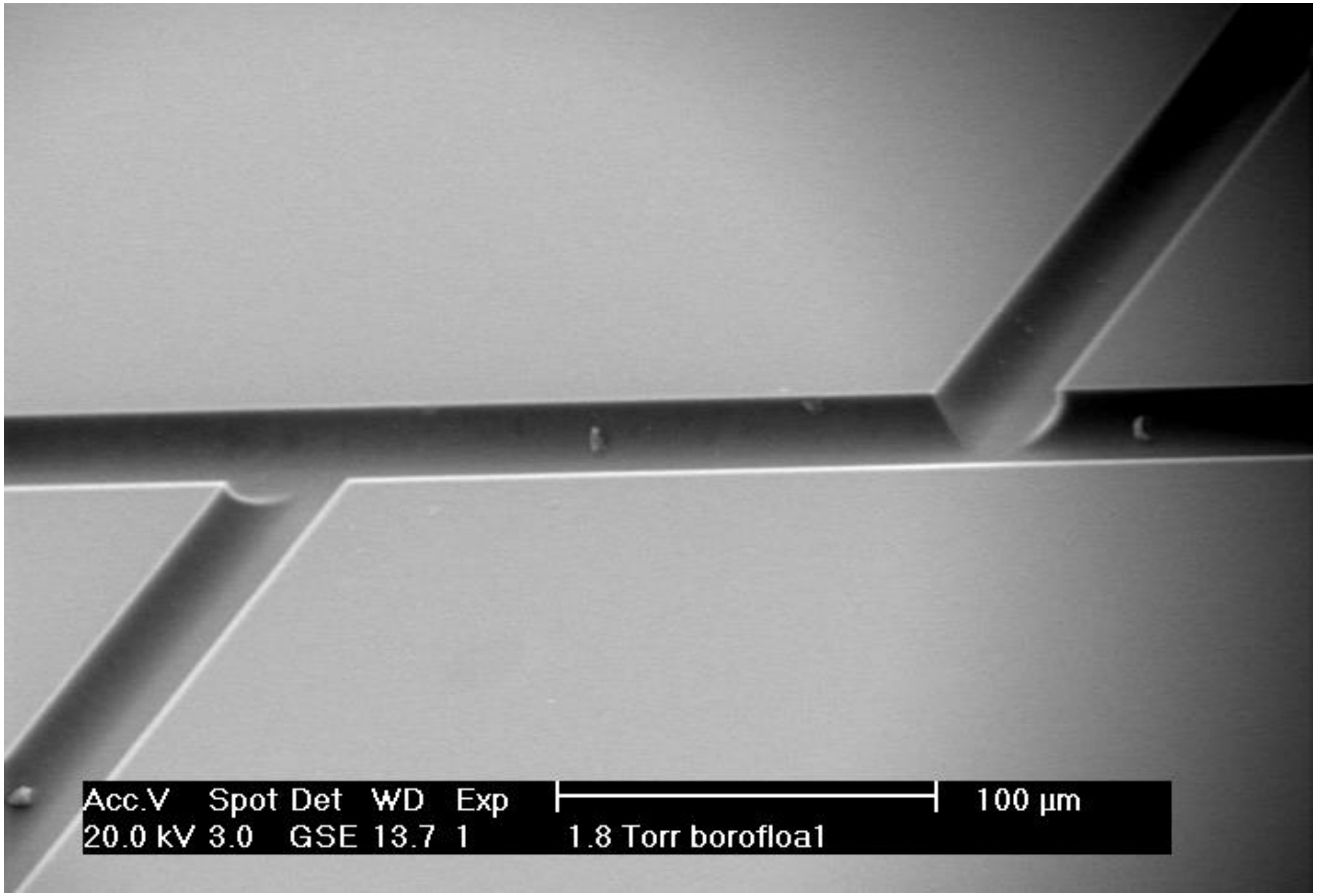




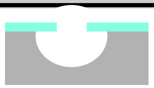
Isotropic Applications: SNOM quartz tips



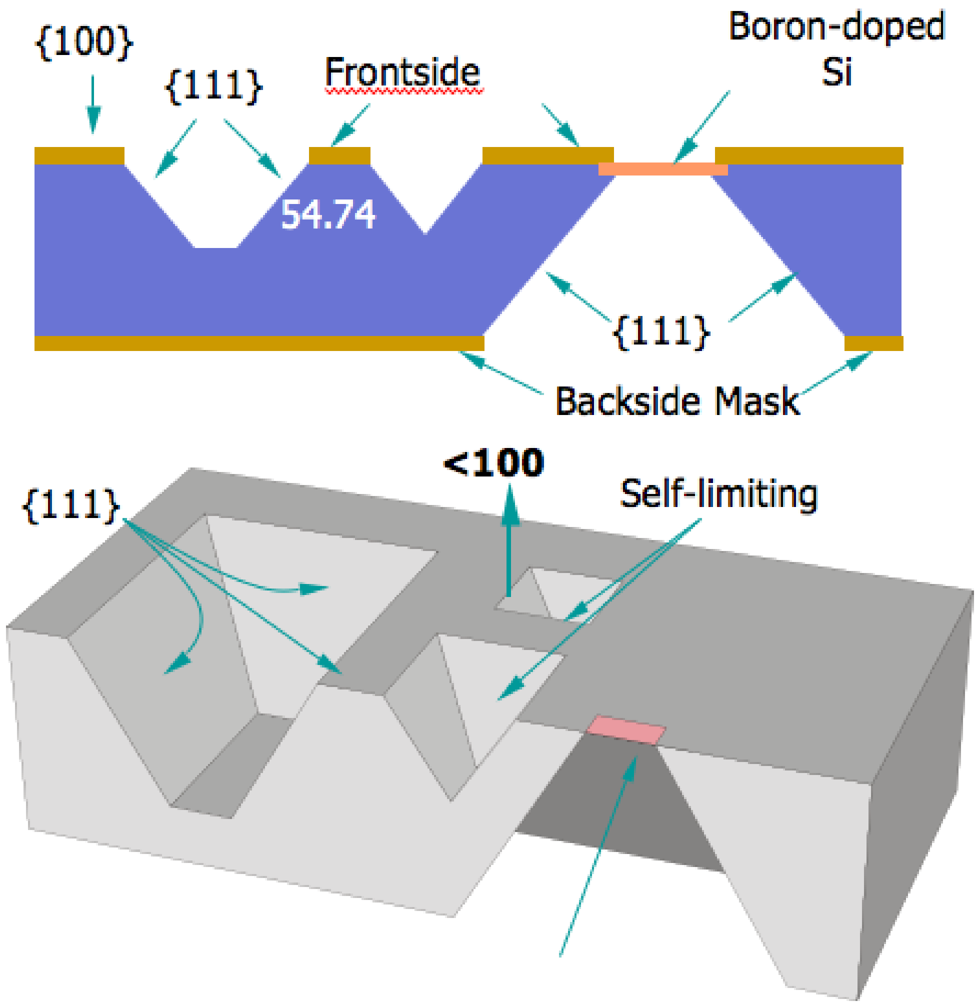
Isotropic Applications: Microchannels in glass



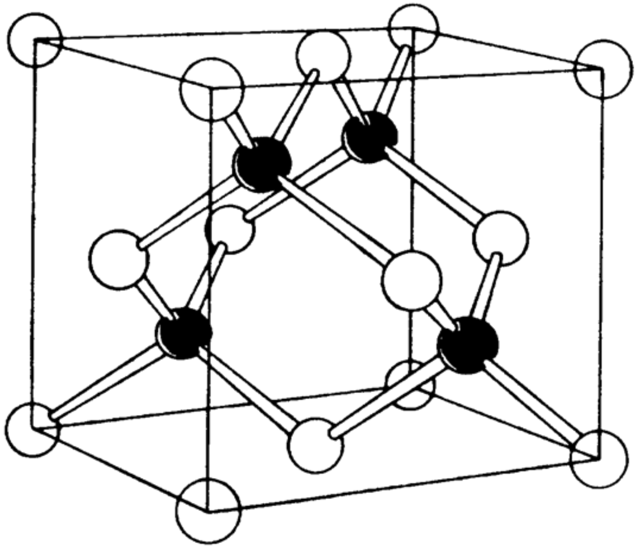
Isotropic Wet Etching – conductors

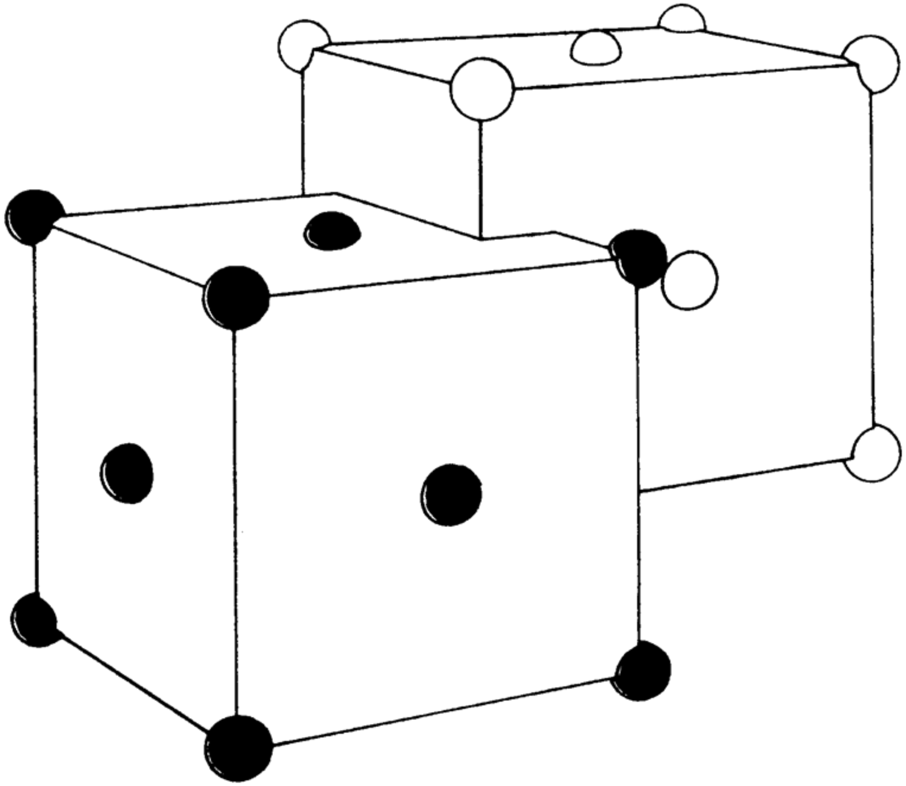


Material	**Etchant**	**Etch rate**
Aluminum	H3PO4 - HNO3	0.15 - 0.25 um/min
Chromium	Ce(SO4)2 - HNO3	0.08 um/min
Copper	FeCl3	50 um/min
Gold	HCl - HNO3	25-50 um/min
Nickel	FeCl3	12-25 um/min
Platinum	HCl - HNO3	0.05 um/min
Silver	HNO3	12-25 um/min
Titanium	HF	12 um/min
Tungsten	KH2PO4, KOH K3Fe(CN)6	0.16 um/min


{100}
{111}
Frontside
Boron-doped Si
54.74
{111}
Backside Mask
{111}
<100
Self-limiting

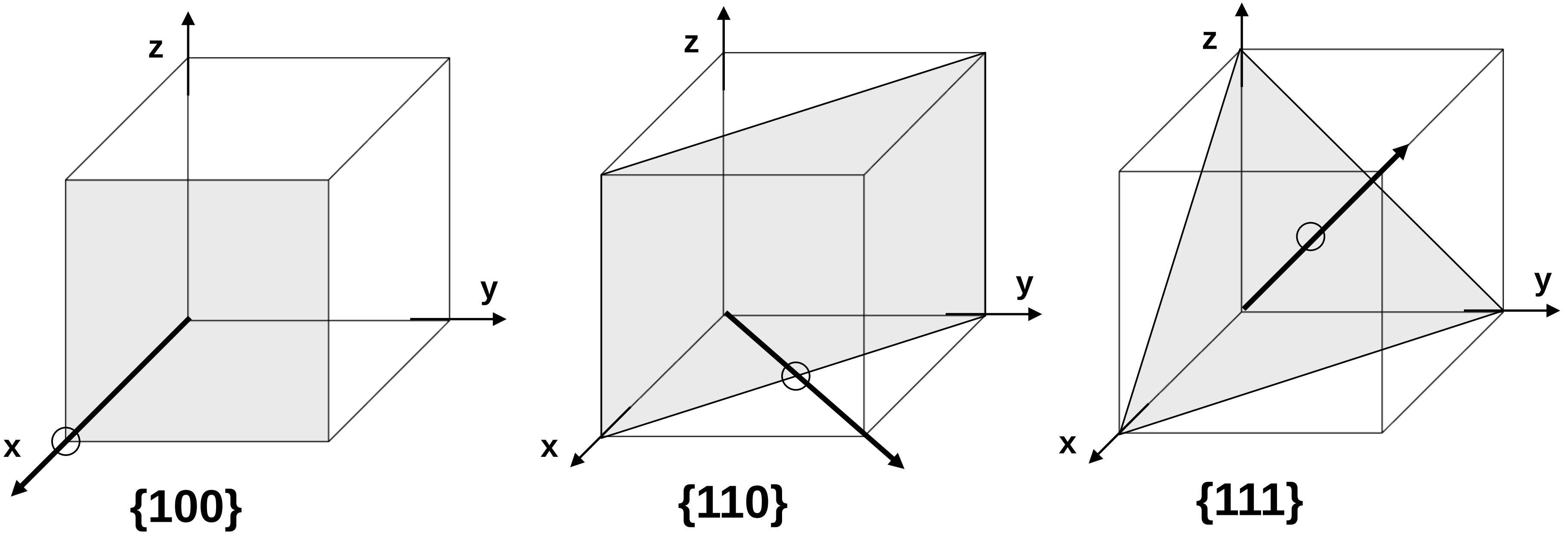
Silicon atomic structure





- covalently bonded structure
- Silicon coordinates itself tetrahedrally
- Face-centered cubic (fcc) structure
- Lattice parameter of 5.4309 Å

Miller indices

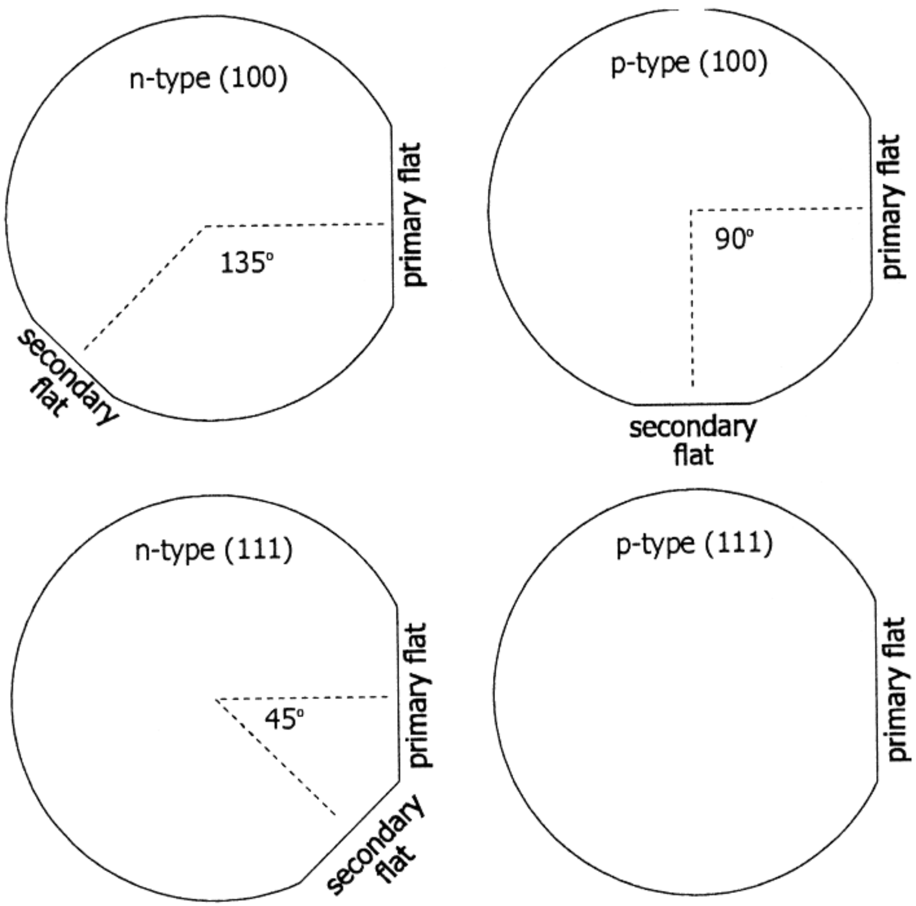


1 / intercept of the vector from origin

Notation: [100] direction, <100> direction family

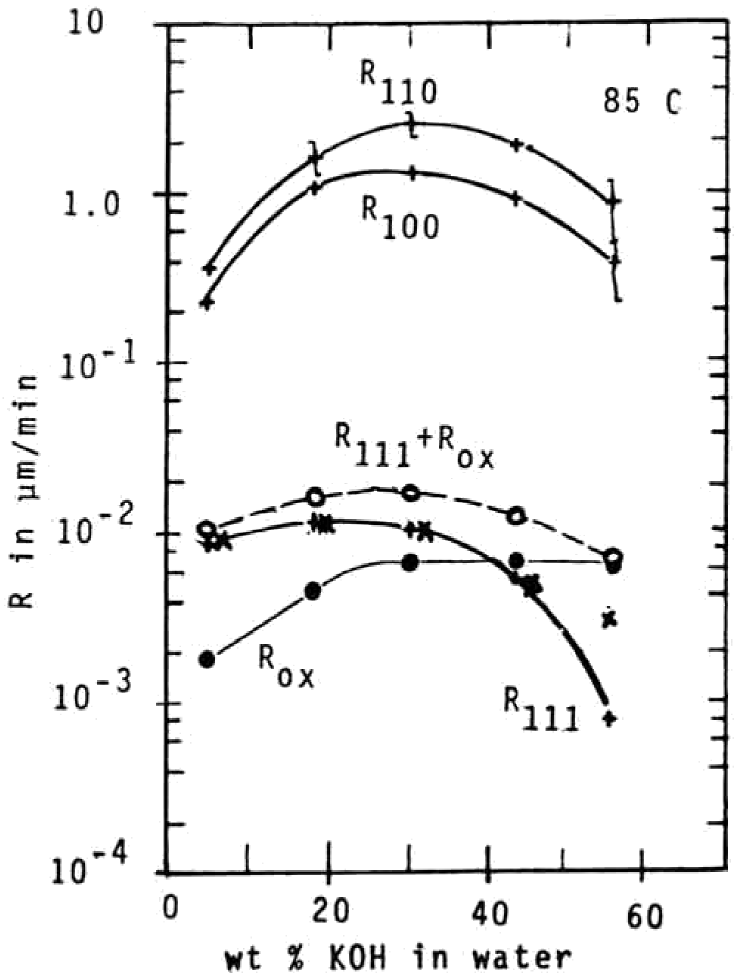
(100) plane {100} plane family

Wafer orientation



KOH etching reaction

- $Si + OH^{-} + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_{2(g)}$
- Masking: Resist will not survive
  oxide is attacked slowly
  Nitride is not attacked
- Etch Rate: {110} > {100} >> {111}
- Used at elevated temperature (50 - 80 ºC)

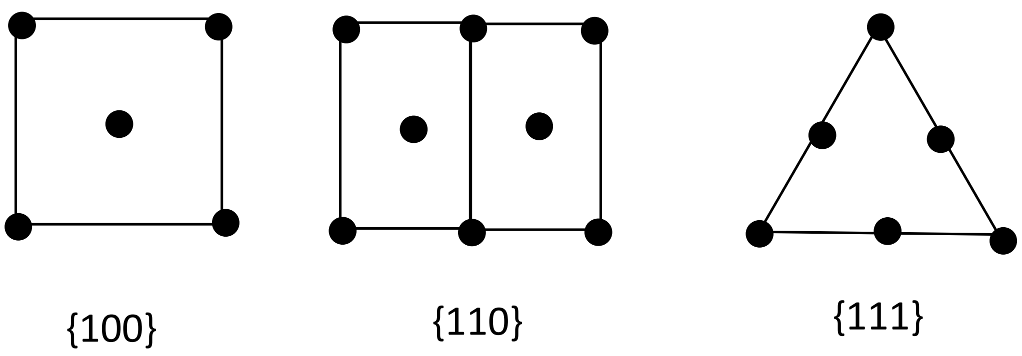


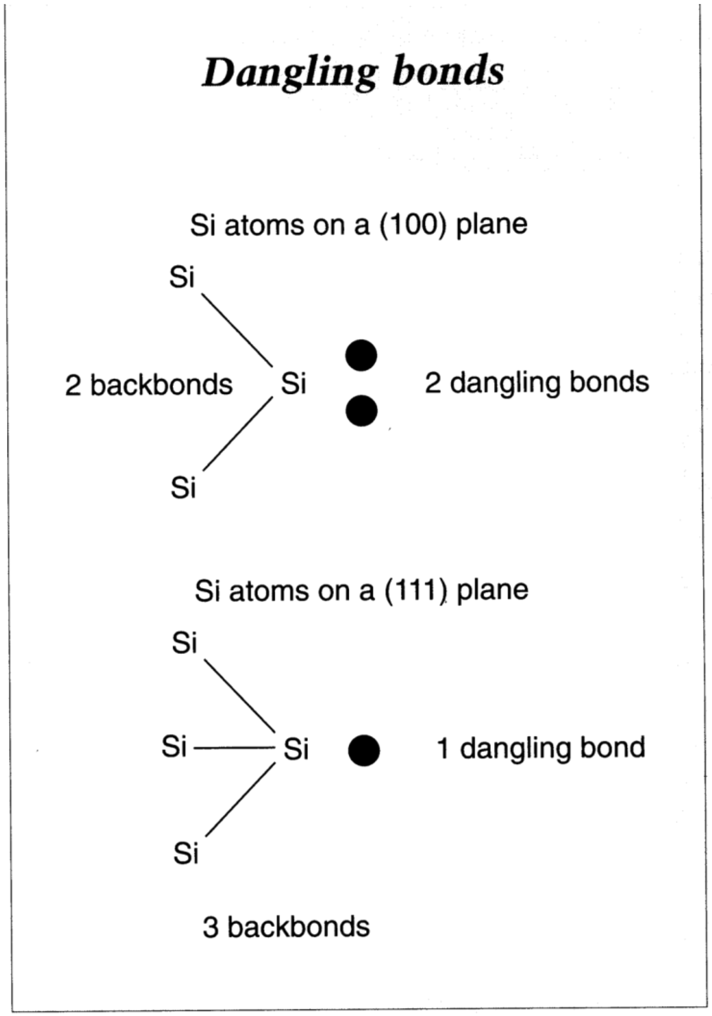
From M. Madou, Fundamentals of Microfabrication, 1997

Anisotropic etching models

- Seidel's et al. model based on the difference in energy levels of backbond-associated surface states for different crystal orientation

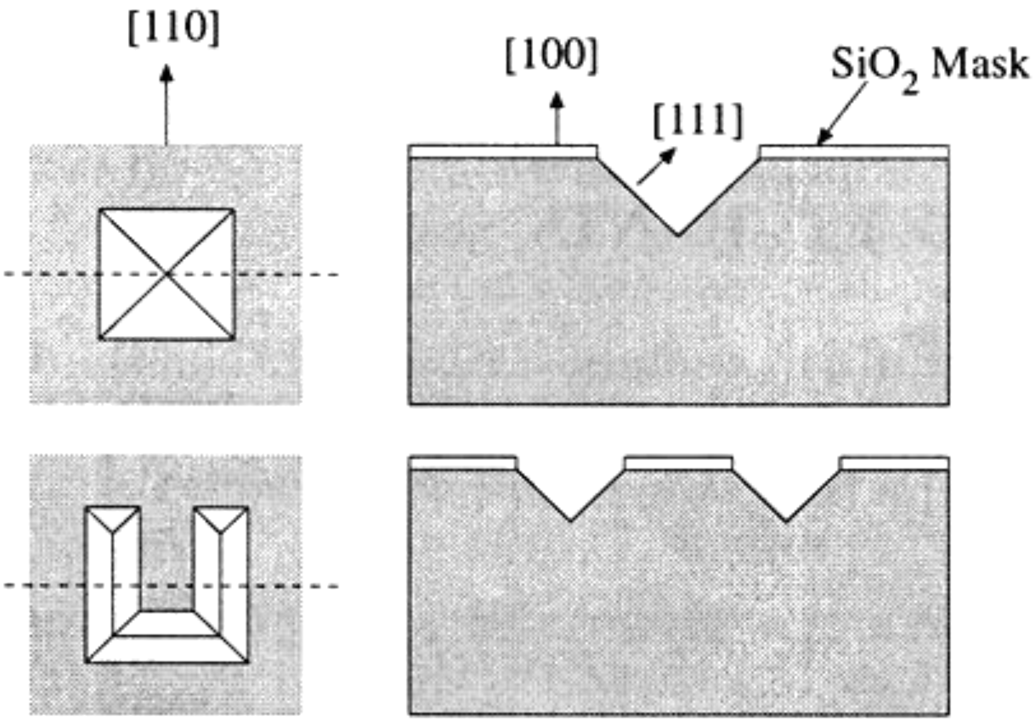
- Density of atoms depends on crystal orientation

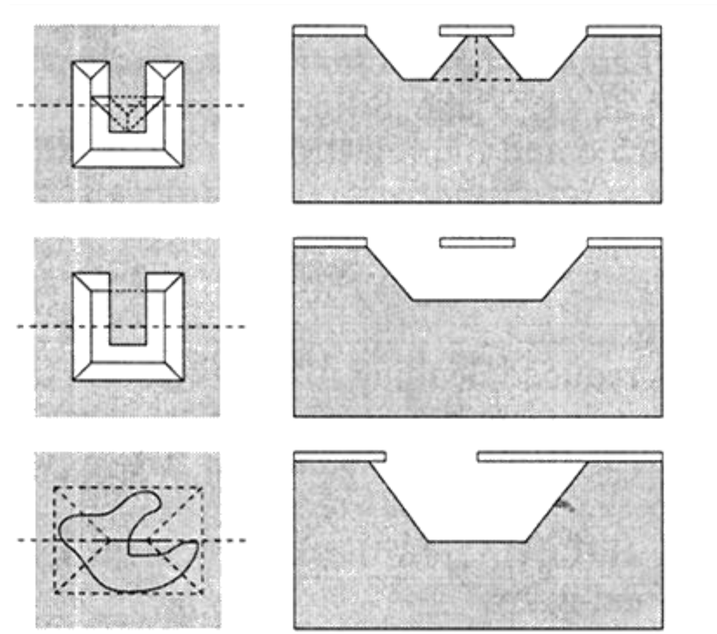




From M. Madou, Fundamentals of Microfabrication, 1997

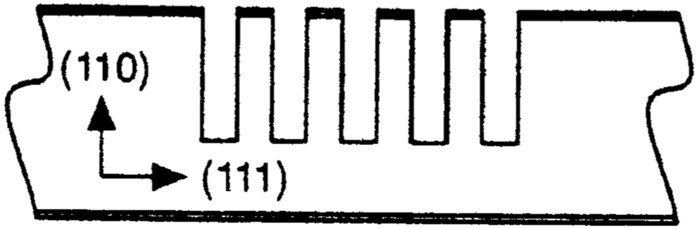
Anisotropic etching: 100 orientation

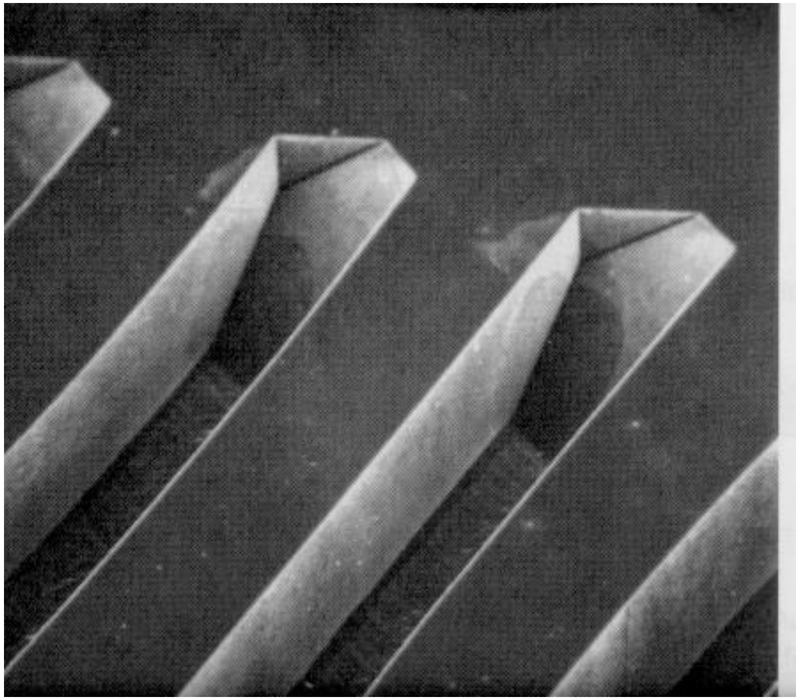




From M. Madou, Fundamentals of Microfabrication, 1997

Anisotropic etching: 110 orientation





From M. Madou, Fundamentals of Microfabrication, 1997

Masking options

- KOH: Si_3N_4, SiO_2
- TMAH: SiO_2, Si_3N_4
- Better protection with thermal SiO_2 than CVD
- Better protection with LPCVD than PECVD

From M. Madou, Fundamentals of Microfabrication, 1997

Etch stop techniques

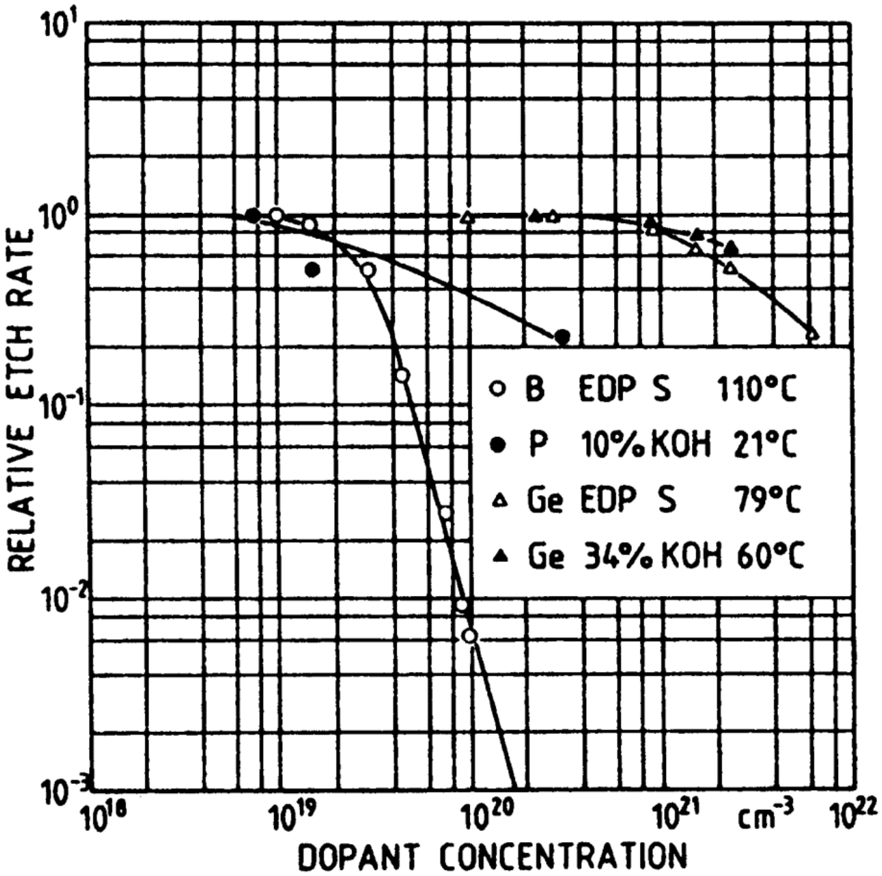
- Non uniformity of wafer thickness
- Variation in etch rates critical for thin membranes
  (< 20 mm Si left)
  ->Time-based technique not suitable
- Etch-stop required to obtain precise Si thickness

From M. Madou, Fundamentals of Microfabrication, 1997

Boron Etch stop

- Anisotropic etchant do not attack boron-doped (p+) Si

=> Diffusion or implantation of boron in high concentration



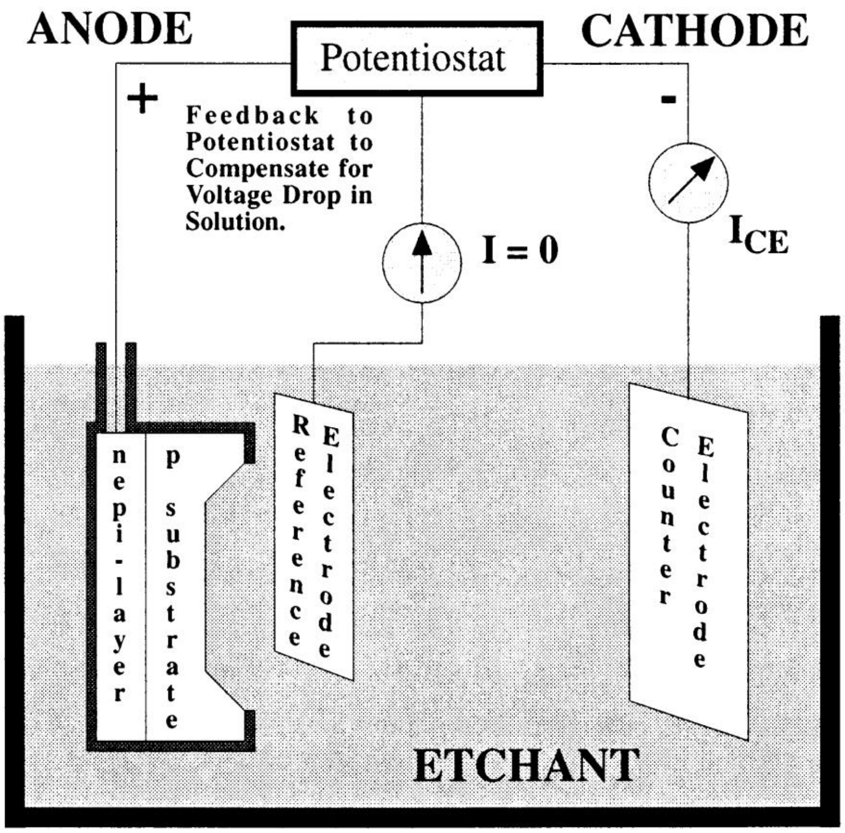
From M. Madou, Fundamentals of Microfabrication, 1997

Electrochemical Etch stop

- Lightly doped p-n junction
- Bias between wafer and counter electrode in etchant

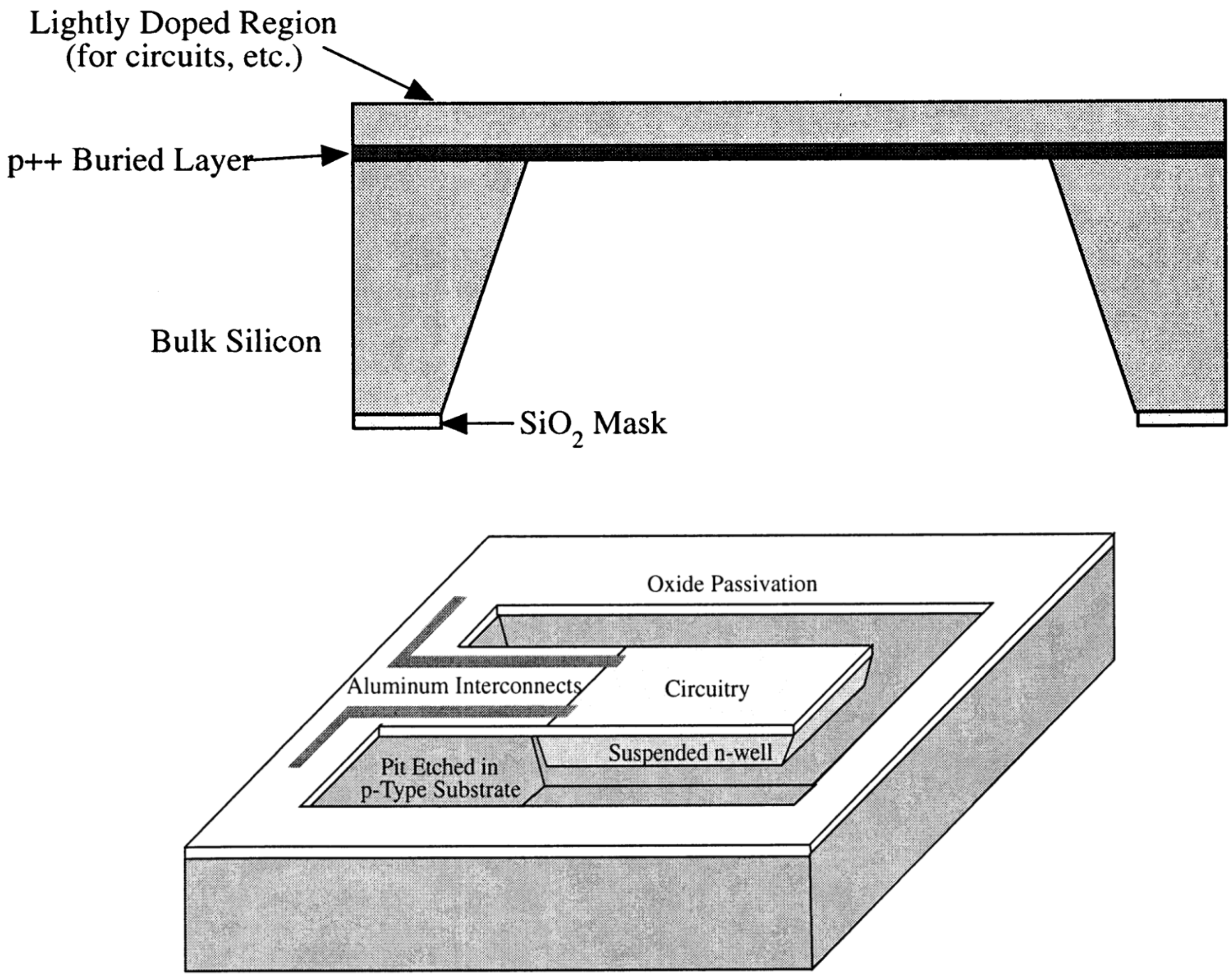
For example:

- Epitaxal growth of n-type layer on a p-type substrate
- p-n junction forms a large diode over the whole wafer
- Wafer in a holder, potential on the n-type epilayer and on the counter electrode



From G.T.A. Kovacs, Micromachined Transducers Sourcebook, 1998

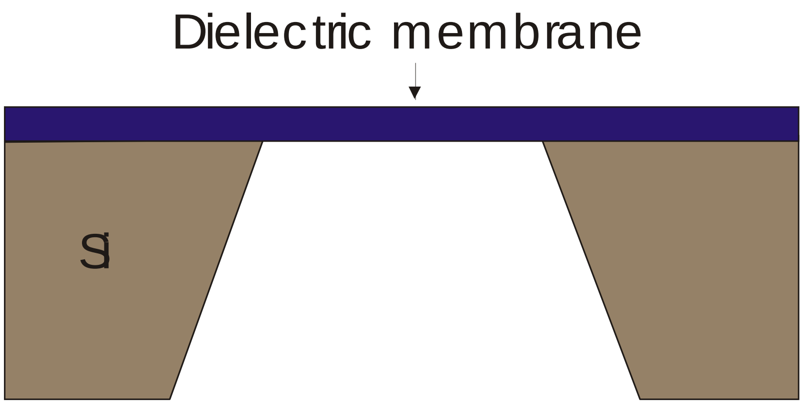
Etch stop structures



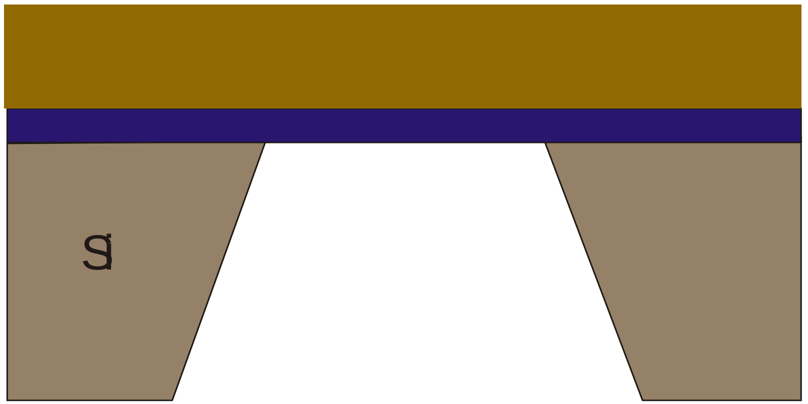
From G.T.A. Kovacs, Micromachined Transducers Sourcebook, 1998

Etch stop structures

- Dielectric masking layer used as etch stop (SiO_2, Si_3N_4)

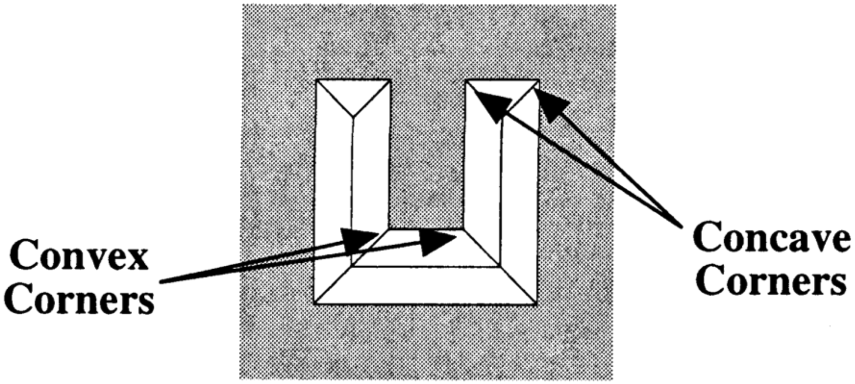


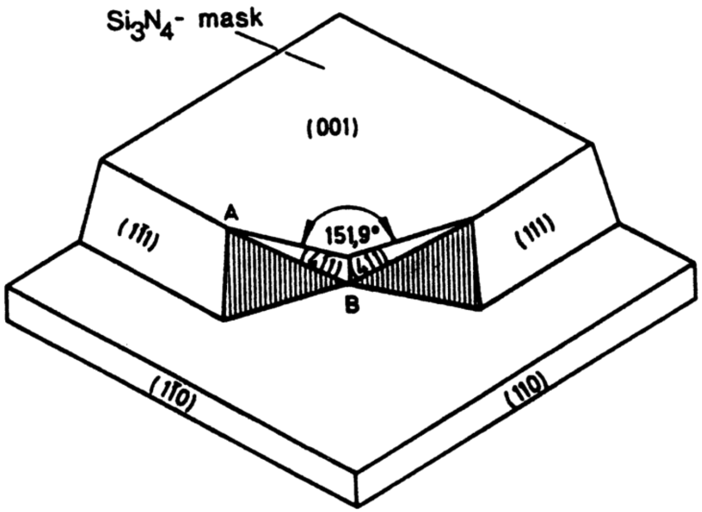
- Silicon On Insulator (SOI) Wafers



Etch compensation structures

- High index and etch rate planes develop at convex corners

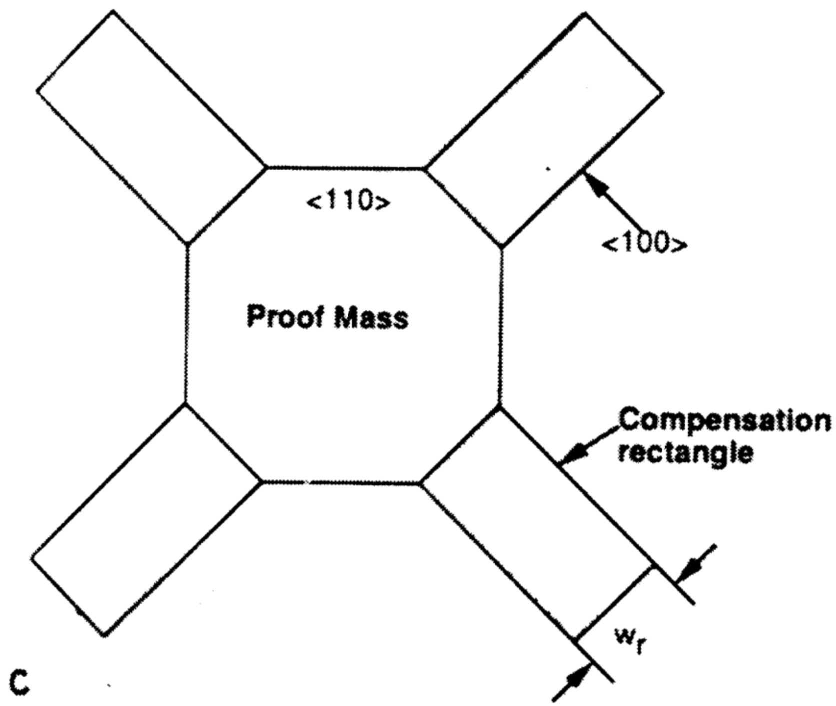


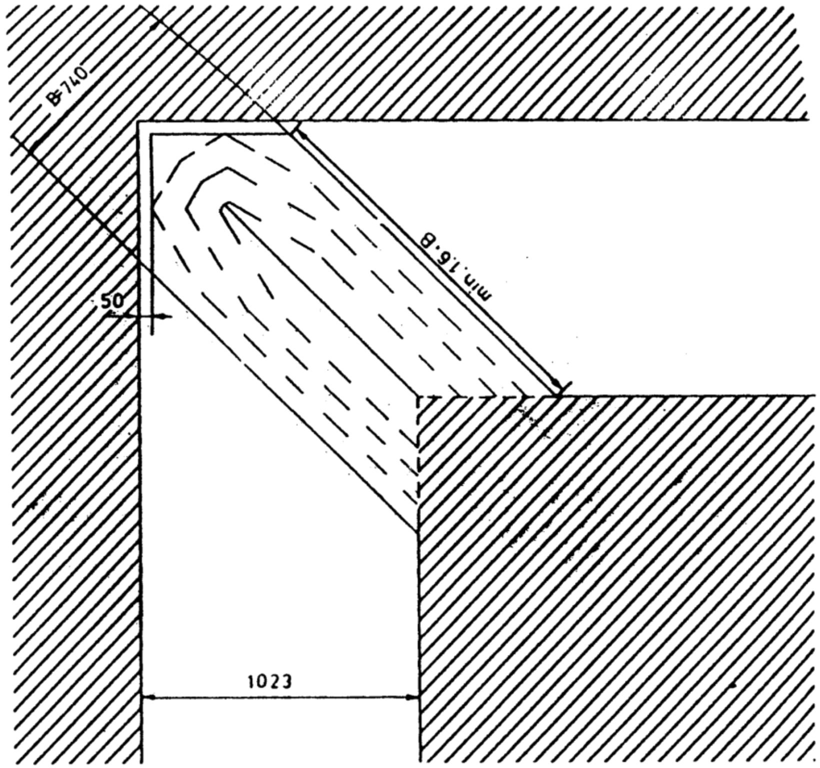


=> Compensation structures required to obtain square Si-masked structures

From M. Madou, Fundamentals of Microfabrication, 1997

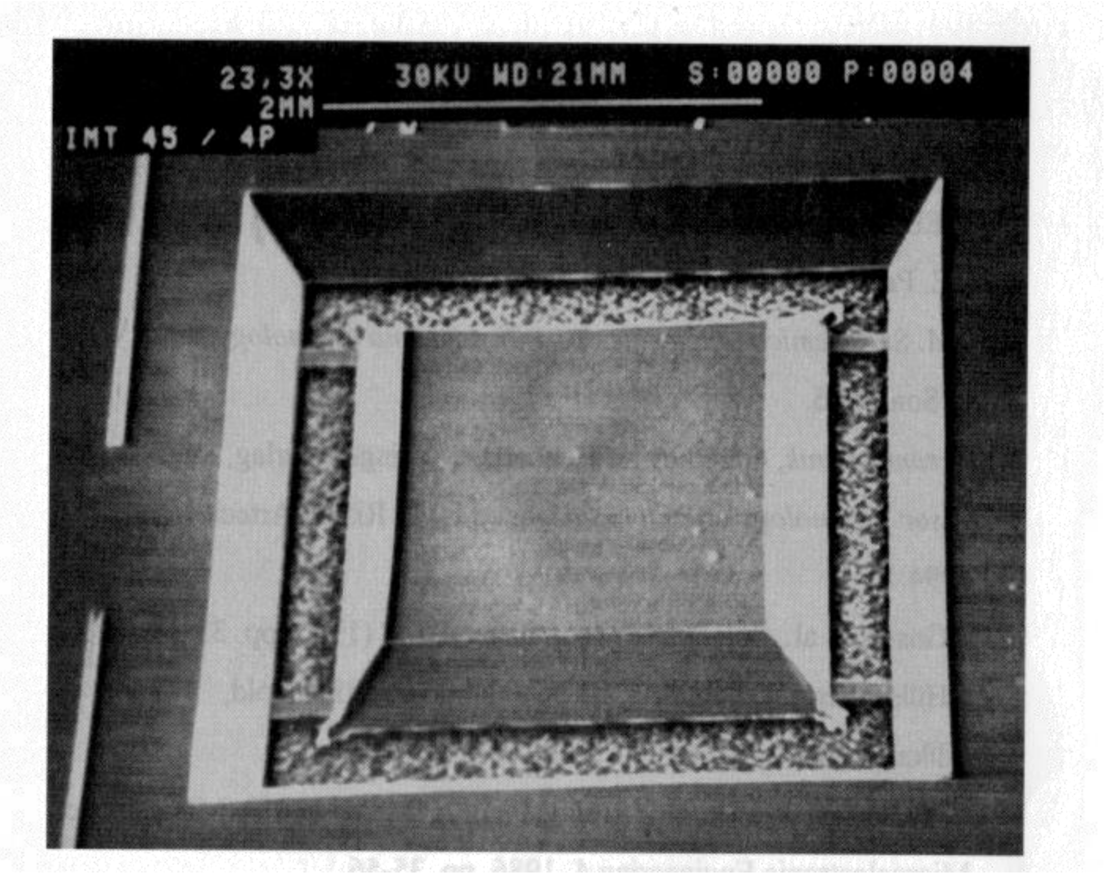
Etch compensation structures





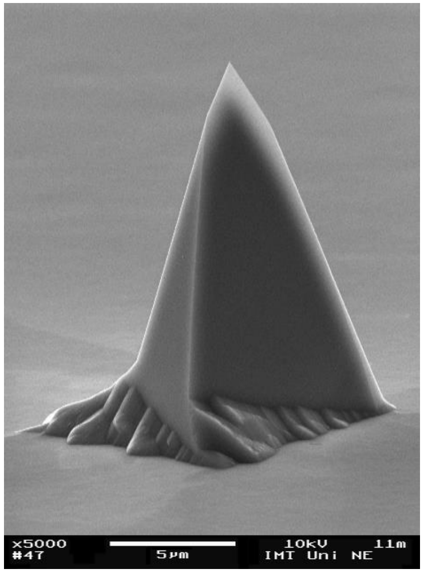
From M. Madou, Fundamentals of Microfabrication, 1997

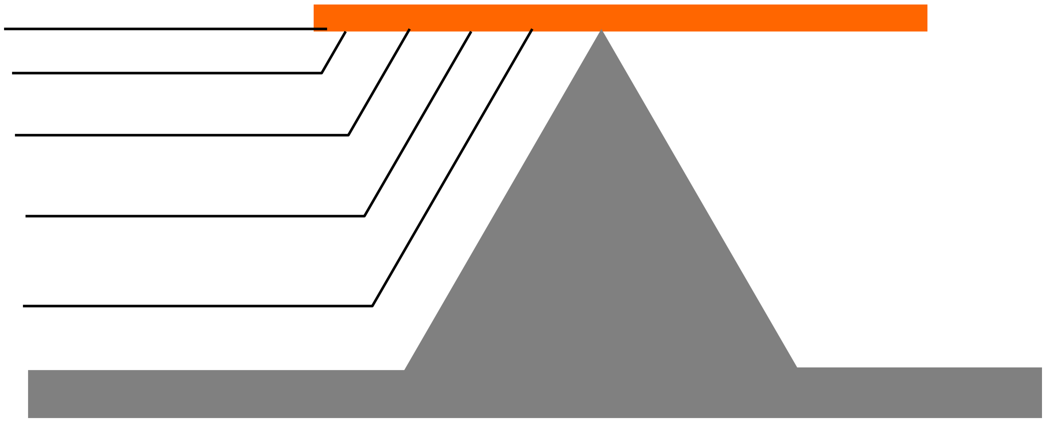
KOH Application: Accelerometer

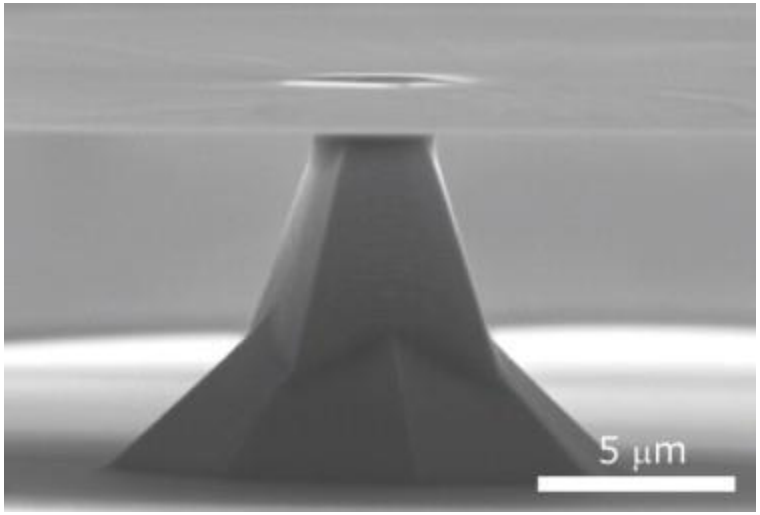


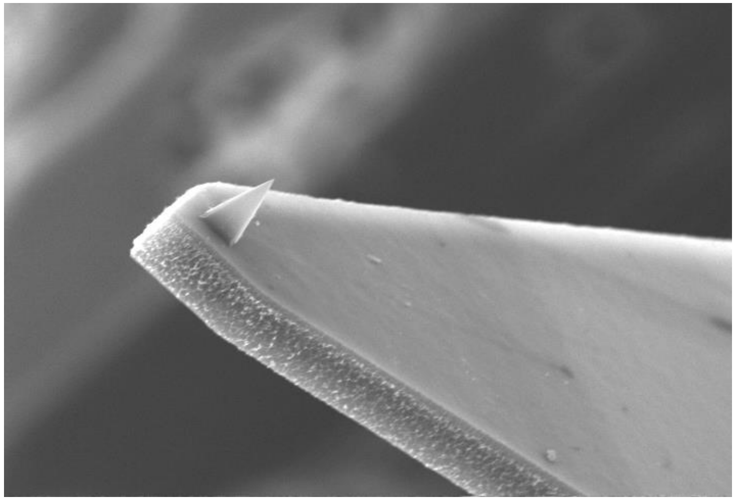
From M. Madou, Fundamentals of Microfabrication, 1997

KOH Application: Silicon AFM Tips

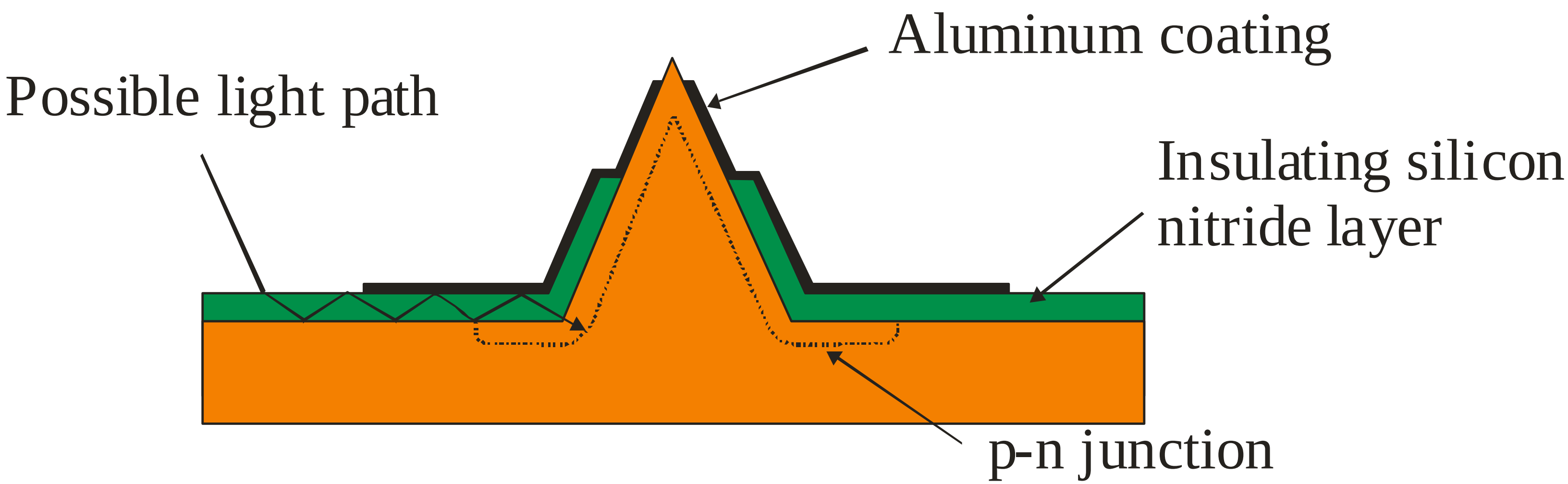




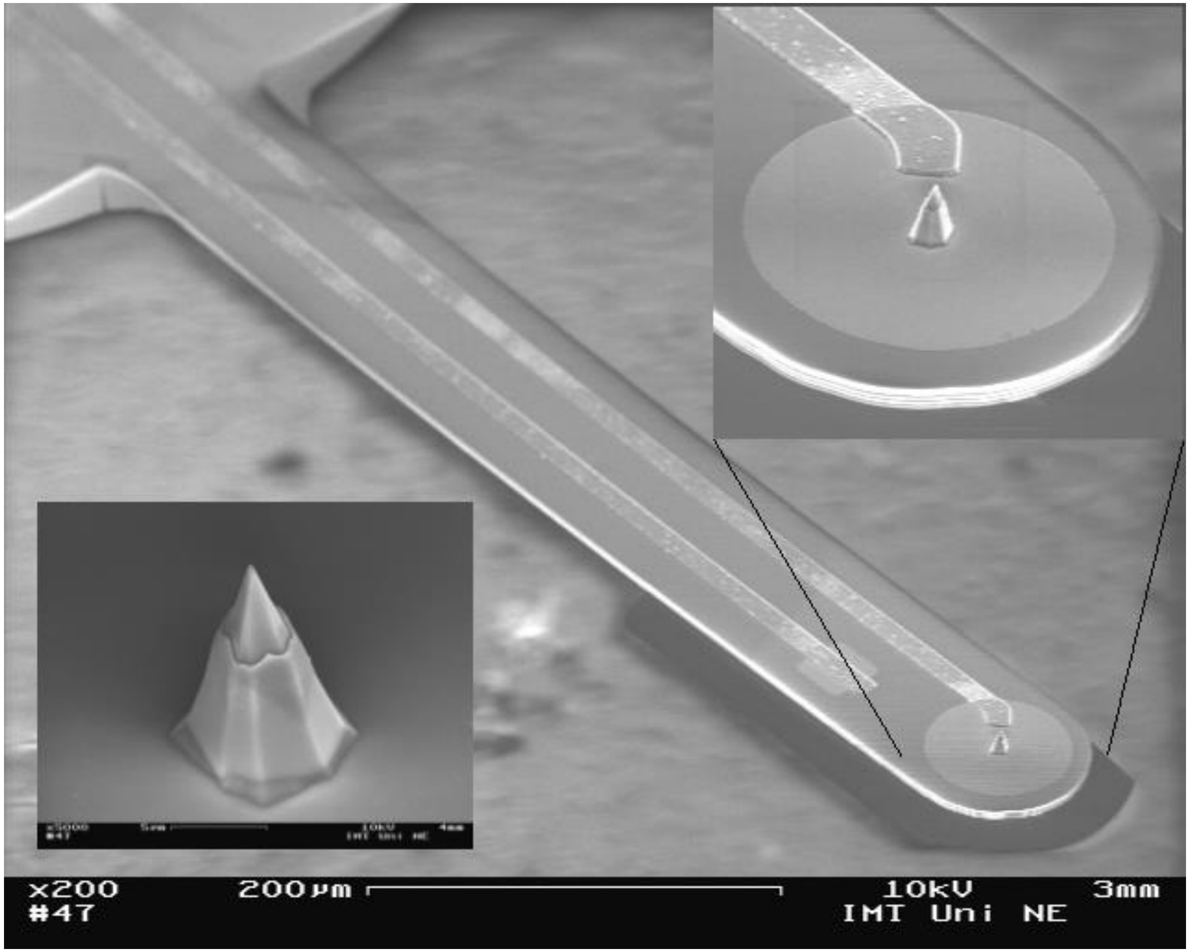




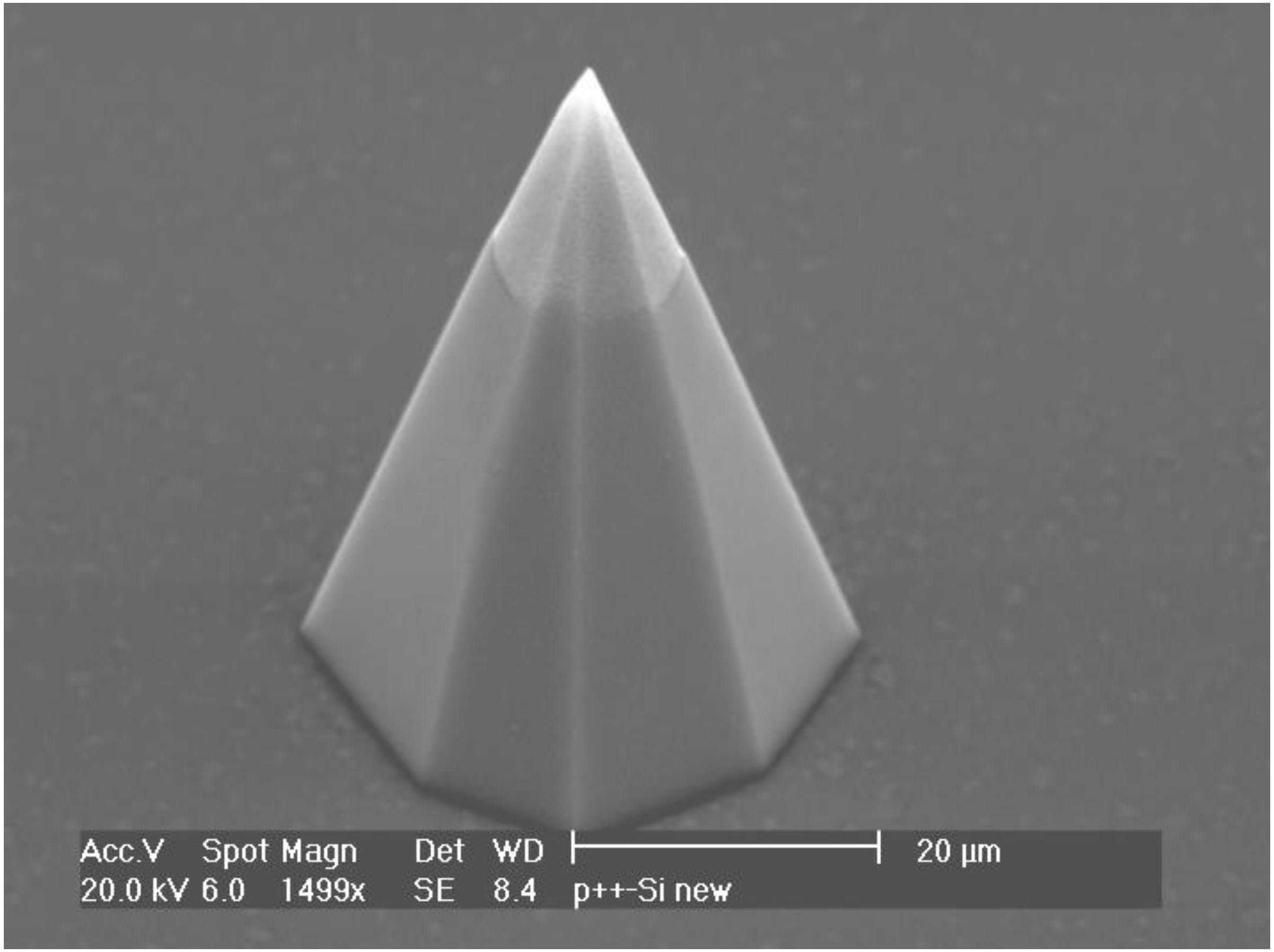
KOH Application: SNOM Tips PN Junction



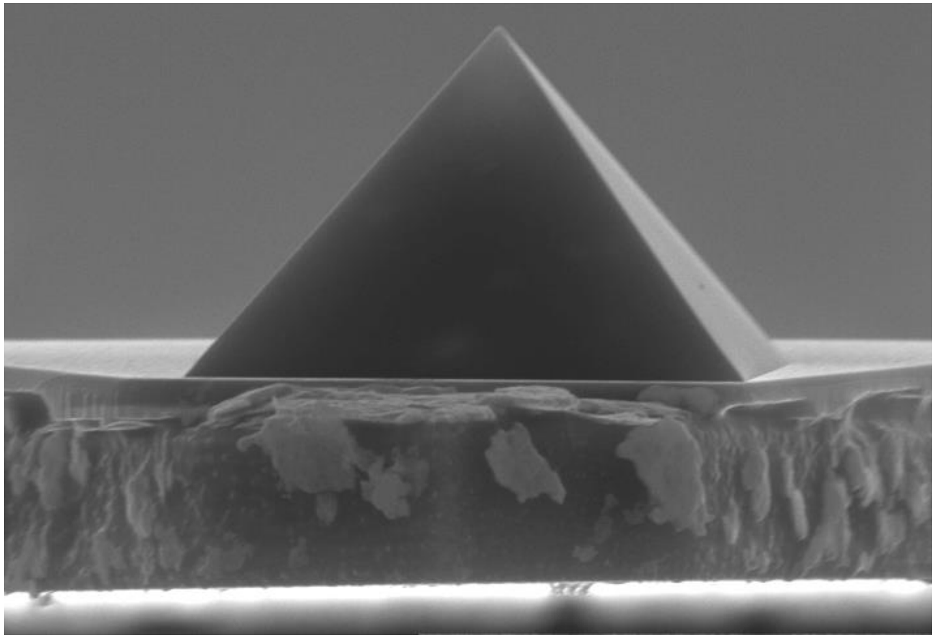
KOH Application: SNOM Tips

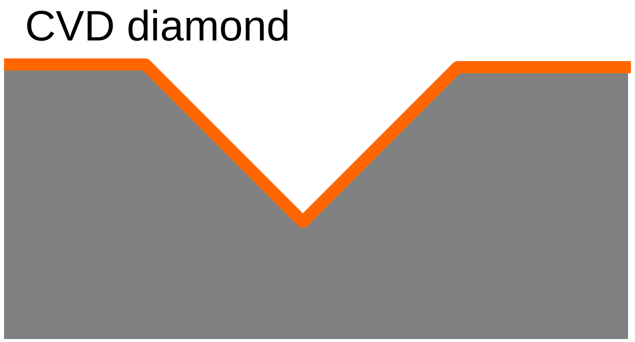


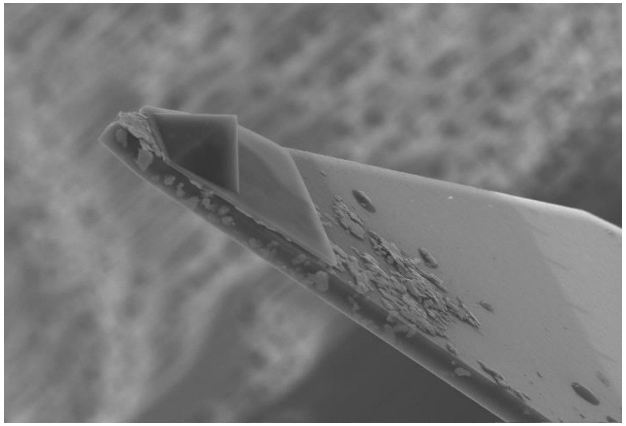
KOH Application: SECM – STM tips



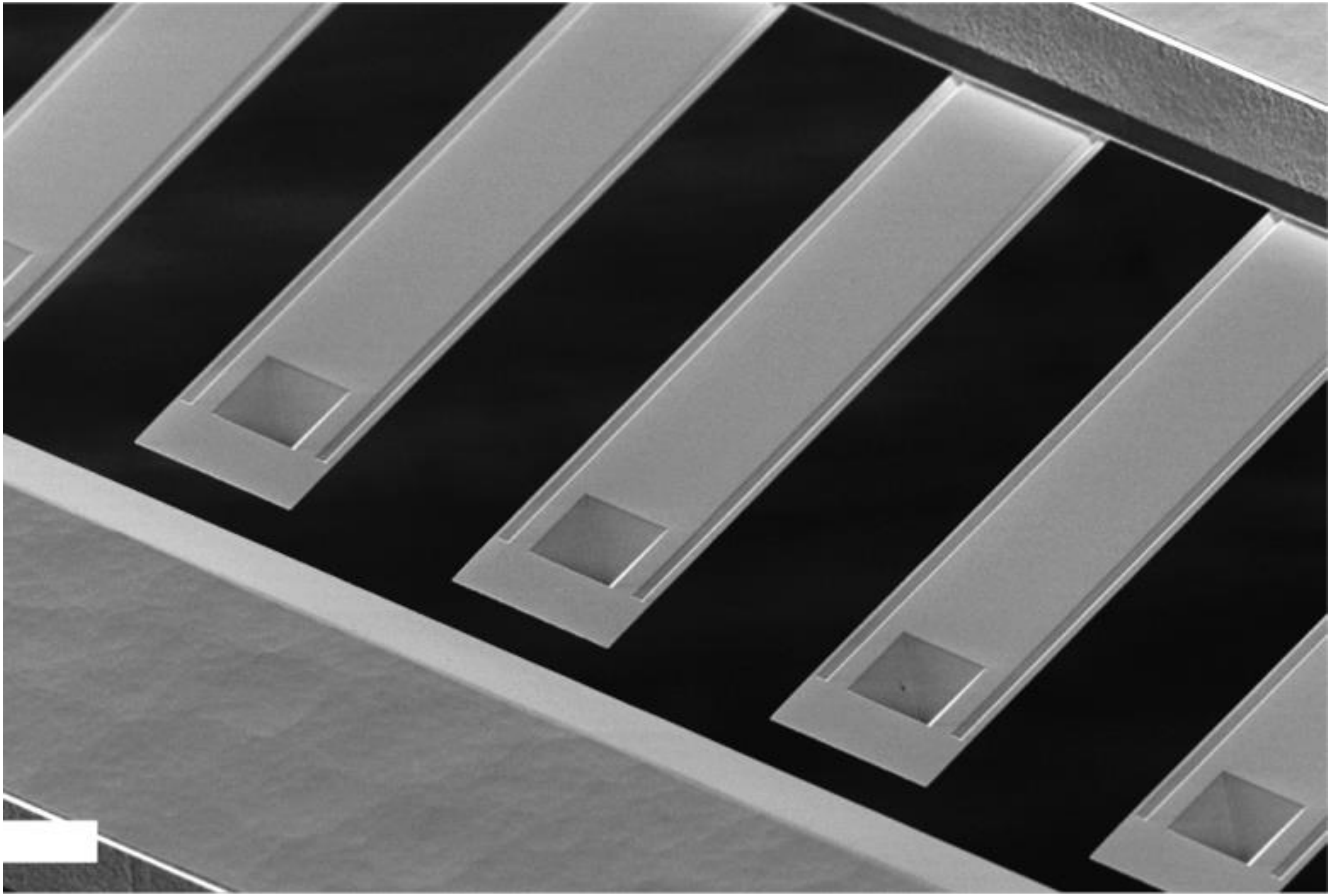
KOH Application: Diamond tips on KOH molds



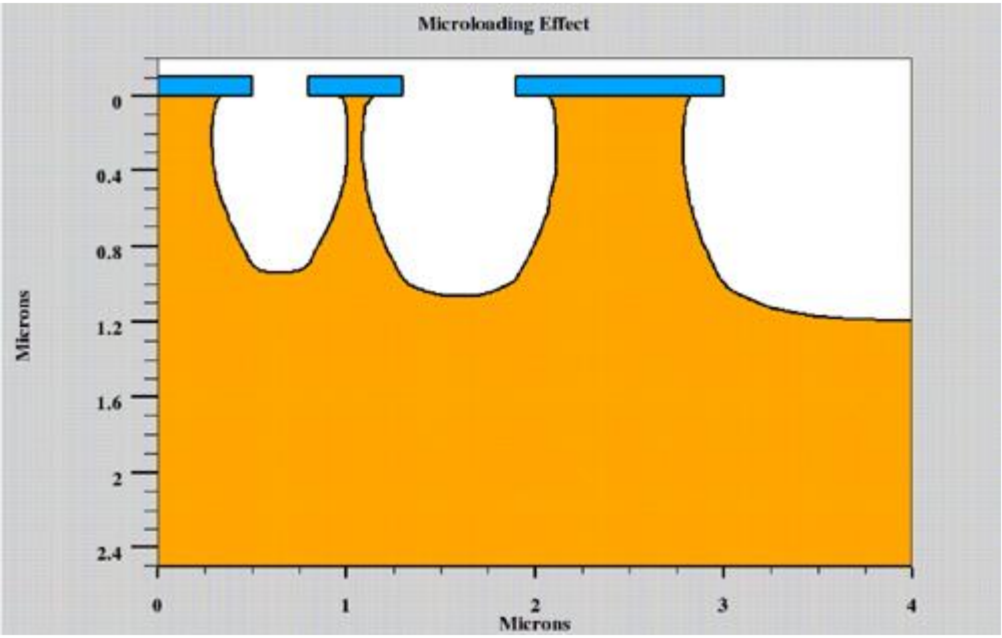




KOH Application: SiNx tips on KOH molds



Bulk Micromachining – Isotropic dry etching (RIE)



Dry etching is the etching of a solid substance by single atoms, radicals, molecules or ions, where the etching particles are in the gas phase or in a plasma. A plasma is a gaseous mixture of free electrons, ions and neutral particles.

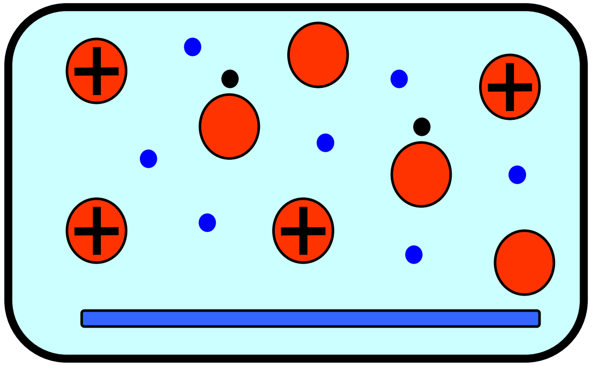
The dry-etching particles are

- not in a liquid
- can move (almost) freely
- the particle movement is defined by
  - the physical boundaries of the etching chamber
  - the electrical and magnetical fields present in the chamber
  - the physical properties of the gas/plasma: pressure and temperature

Non-reactive (chemically)

atoms, molecules

electrons



Reactive:

radical
(an atom with a free valence electron)

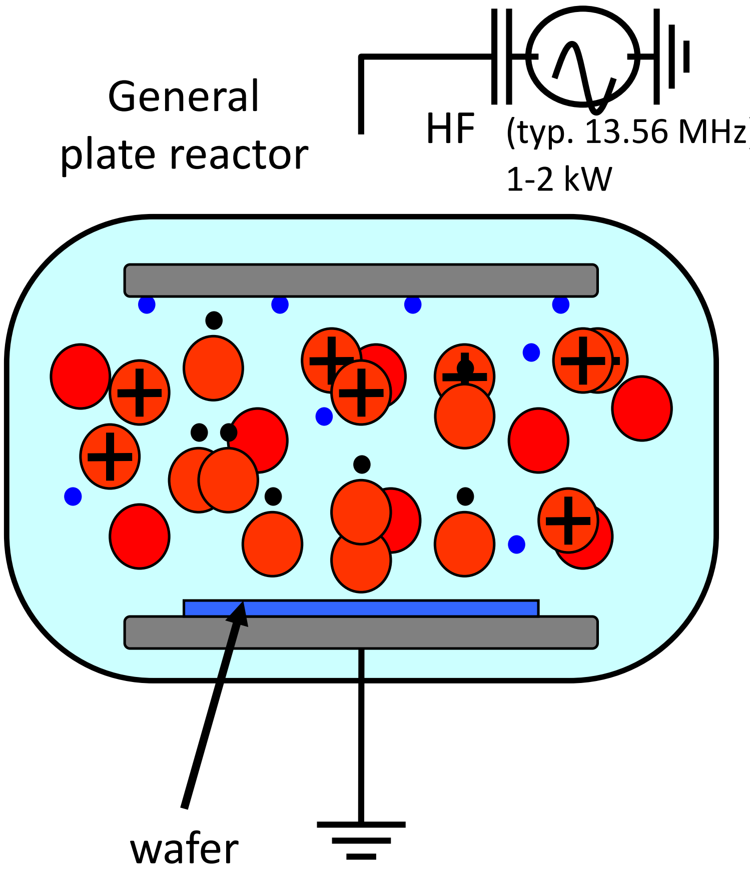
ions

Dry etching **has the following characteristics:**

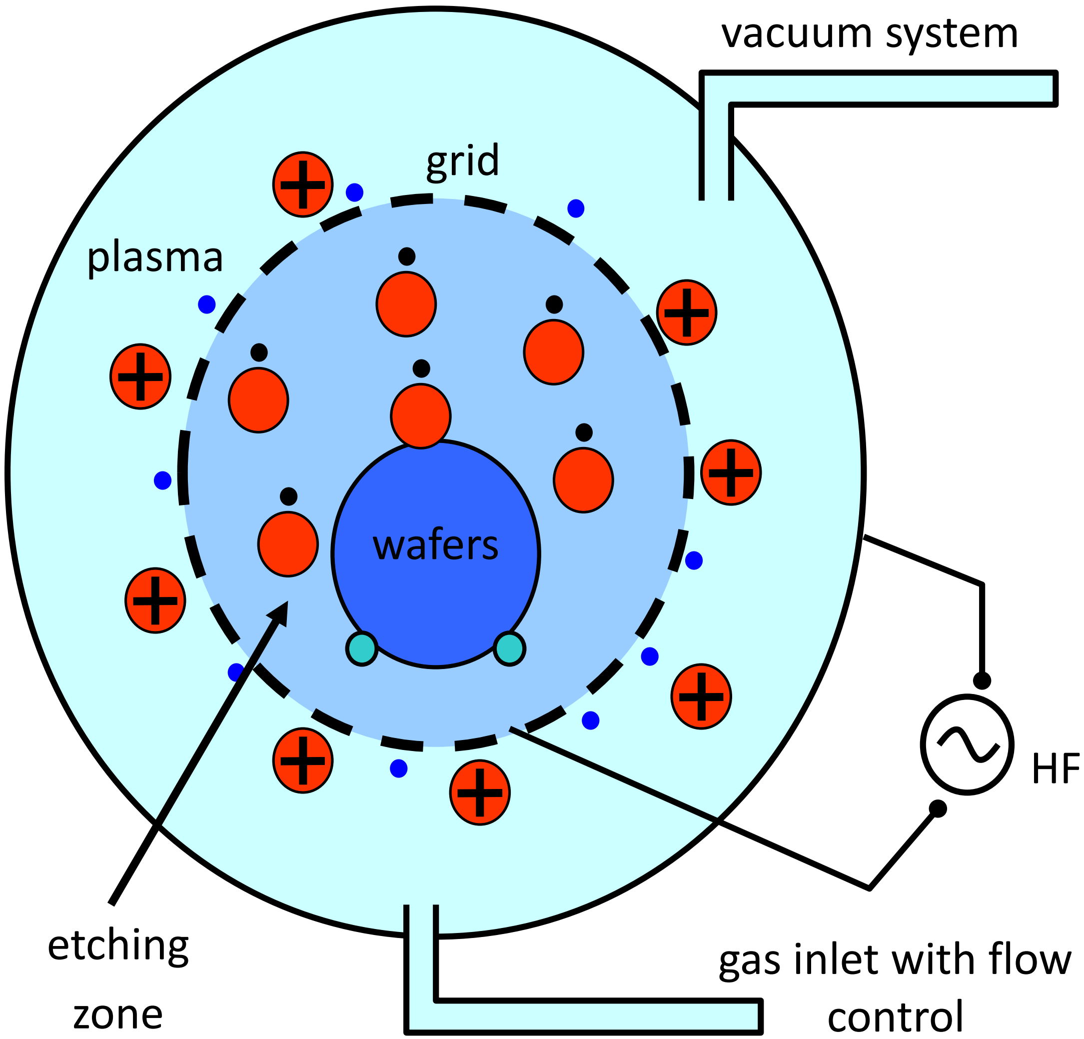
- High reproducibility
- Homogeneous etch rate over wafer
- All materials used in microtechnology can be dry etched
- Sufficient etch selectivity between different materials
- Etch selectivity can be changed by process parameters
- Isotropic and anisotropic etching is possible
- Special processes (DRIE) allow the etching of very steep almost vertical trenches
- Photoresist can be used as a mask (which can be removed by dry etching as well)
- No rinsing in de-ionizes (DI) water is necessary
- Mechanically sensitive structures are not subjected to liquid flows/pressure
- Single-sided etching

How to Create Dry Etching Particles?

1. An electrical neutral gas in a metal chamber
2. The gas pressure (e.g. 5 Pa) is low in the chamber, i.e. the mean free path length of the particles is in the order of the chamber dimensions
3. Applying an alternating electrical field at high frequency (HF at 13.56 MHz) to the gas, which does not interfere with radio
4. The gas molecules are accelerated
5. The gas particles/molecules collide with each other
6. Ionized molecules/atoms and radicals are formed
7. The ions are less mobile than the electrones, which moves the electrones away from the ions
8. An electrical field builds up in the chamber, which accelerates the ions towards the cathode as well
9. The radicals can move freely and are highly reactive
10. The movement and reactivity of the particles can be controlled by pressure, temperature and HF power



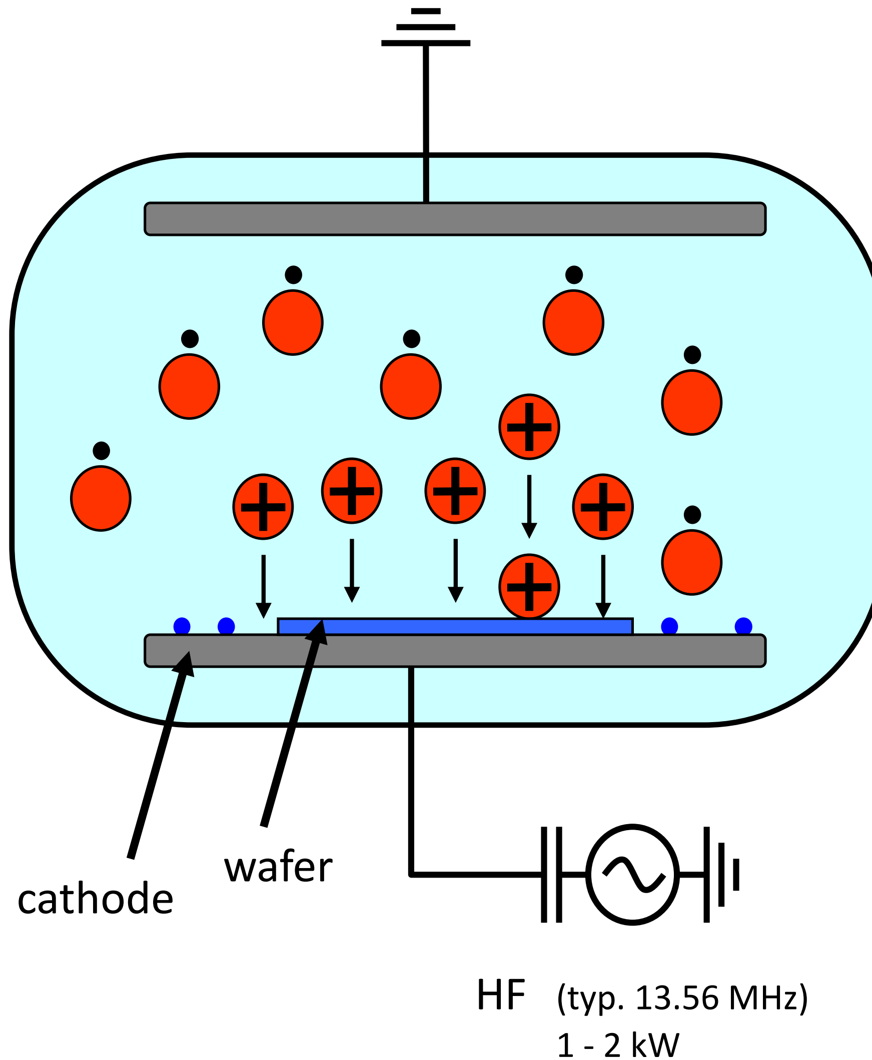
Plasma etcher



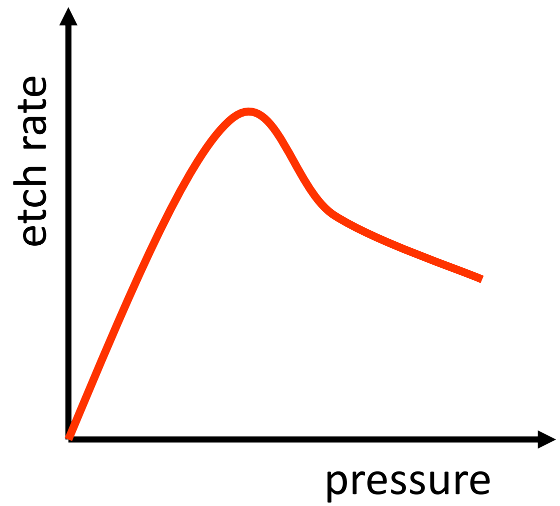
- The HF field is applied to the outer chamber and the grid inside the chamber.
- The electrons and ions are caught by the grid.
- Only the electrical neutral radicals can fly through the grid and enter the etching zone.
- The wafers are etched only by the radicals.
- The etching is purely chemical.
- This etching is mostly used for removing photoresist (photoresist stripping).

Bulk Micromachining – Isotropic dry etching (RIE)

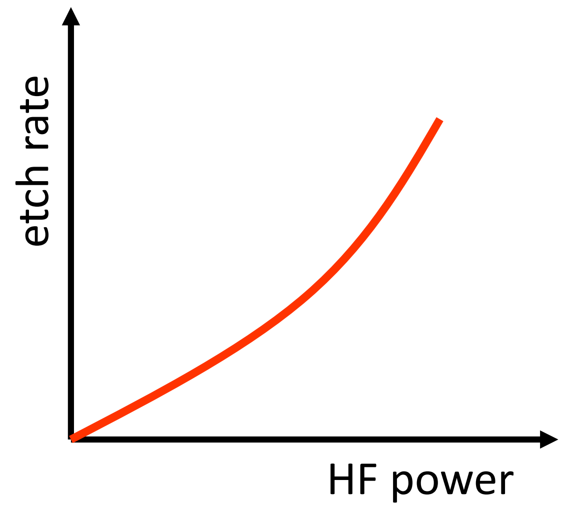
- The HF field is applied to the cathode.
- The wafers are laying on the cathode.
- The ions are accelerated towards the cathode and the wafers.
- Ions and radicals are etching.
- The etching is highly directional, i.e. very anisotropic (vertical walls).
- The etching is chemical and physical (sputter etching by momentum transfer).
- Increasing the pressures leads to a reduces mean free path length of the particles. The particles loose kinetic energy. The etching becomes more chemical and less anisotropic.
- Radicals can bind or etch the etch products of the wafer. No redeposition of materials.



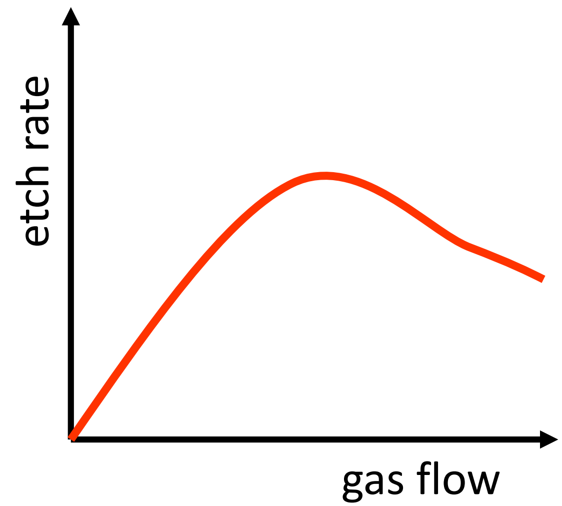
Etch Parameters



- at low pressure only a few reactants are available → low etch rate
- higher pressure means more radicals
- too high pressure reduces the mean free path length → less kinetic energy/particle → physical etch rate lowers



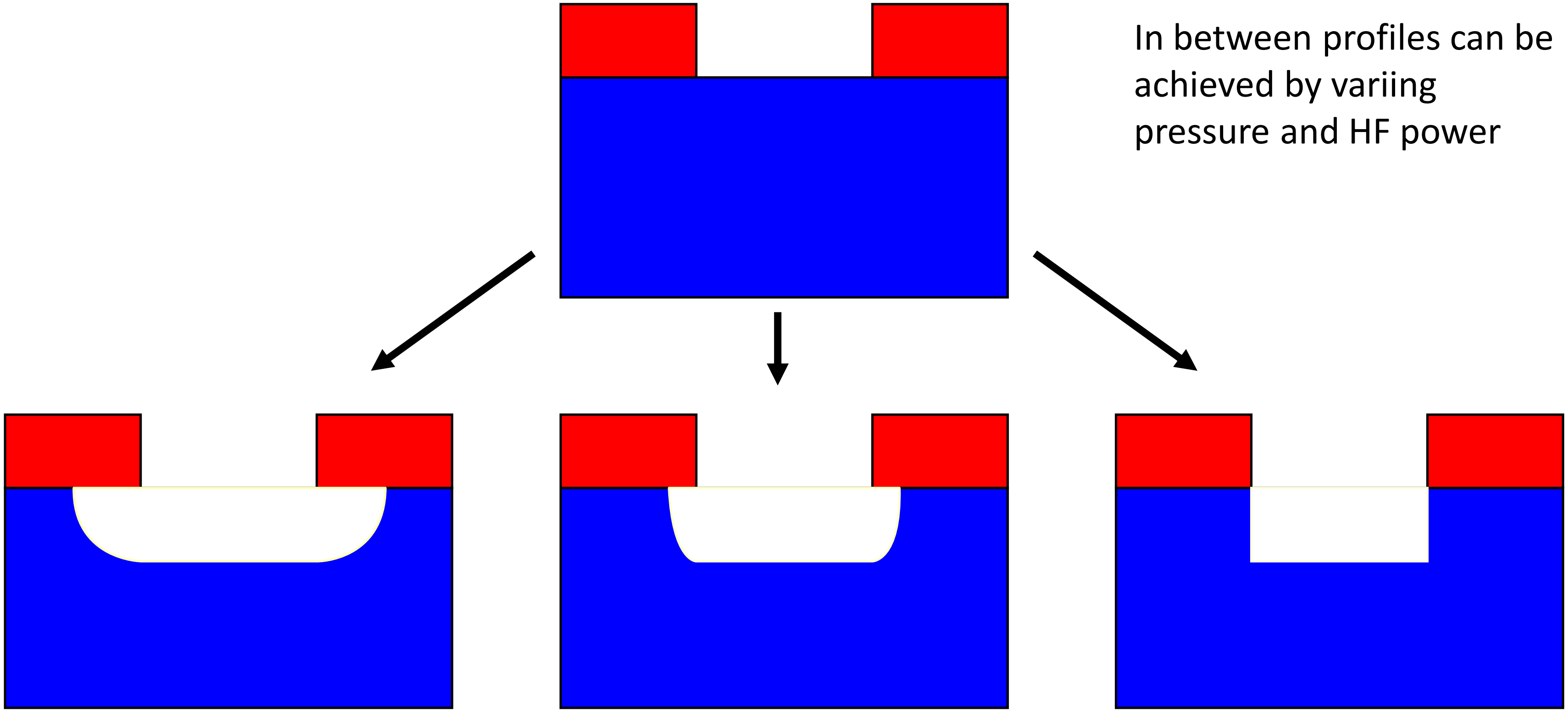
- higher HF power means more particles are ionized and dissociated
- the degree of ionizaion is always smaller than 100%, an more power can hence always create more radicals and ions



- the influence of the gas flow is the same like the pressure dependance
- too little gas → no reactants available
- too much gas → the density of particles is too high

Etch Profiles

In between profiles can be achieved by variing pressure and HF power

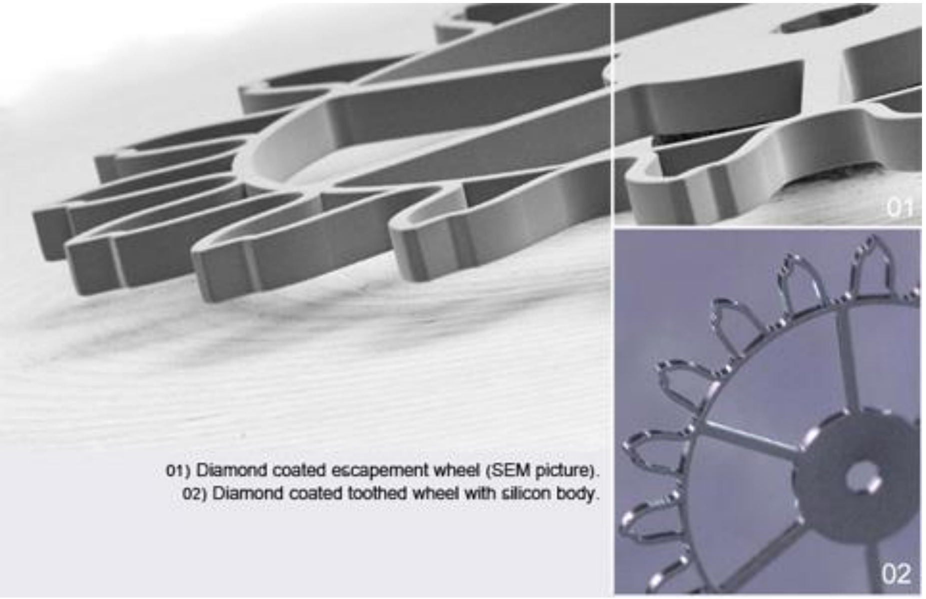


isotropic etch
- chemical etch
- vertical rate = horizontal rate

directional etch
- chemical and physical
- vertical rate > horizontal rate

vertical etch
- mostly physical
- vertical rate >> horizontal rate

Bulk Micromachining – Anisotropic dry etching (DRIE)



01) Diamond coated escapement wheel (SEM picture).
02) Diamond coated toothed wheel with silicon body.

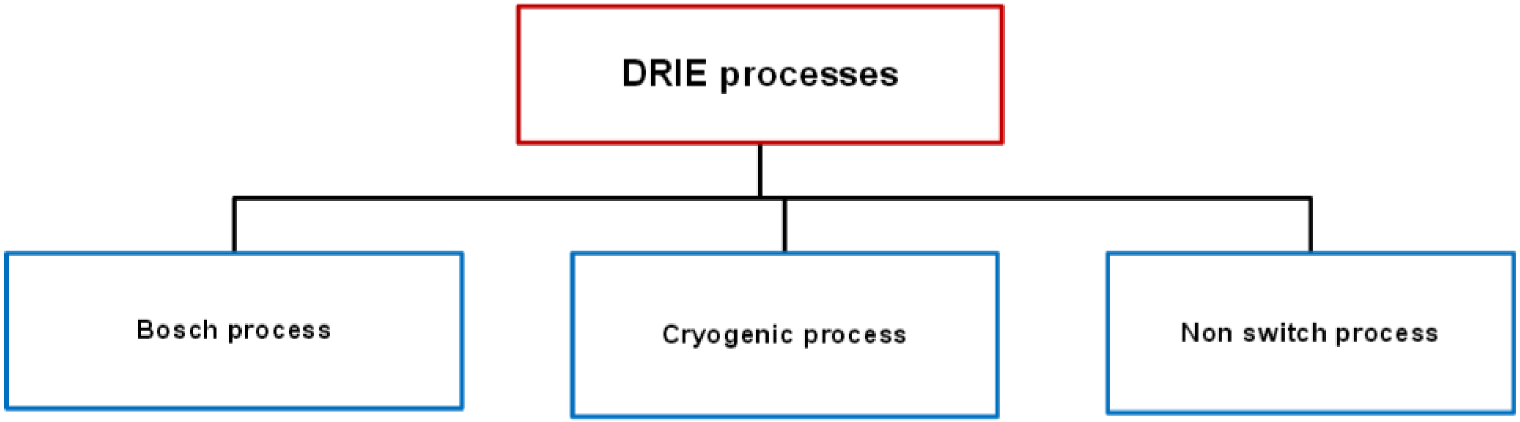
Bulk Micromachining – Anisotropic dry etching: DRIE

- Deep Reactive Ion Etch (DRIE) is a highly anisotropic etch process used to create deep, steep-sided holes and trenches in wafers, with aspect ratio of 20:1 or more.

- It belongs to the RIE group, reactive ion etching group which combines both chemical and physical etching techniques.

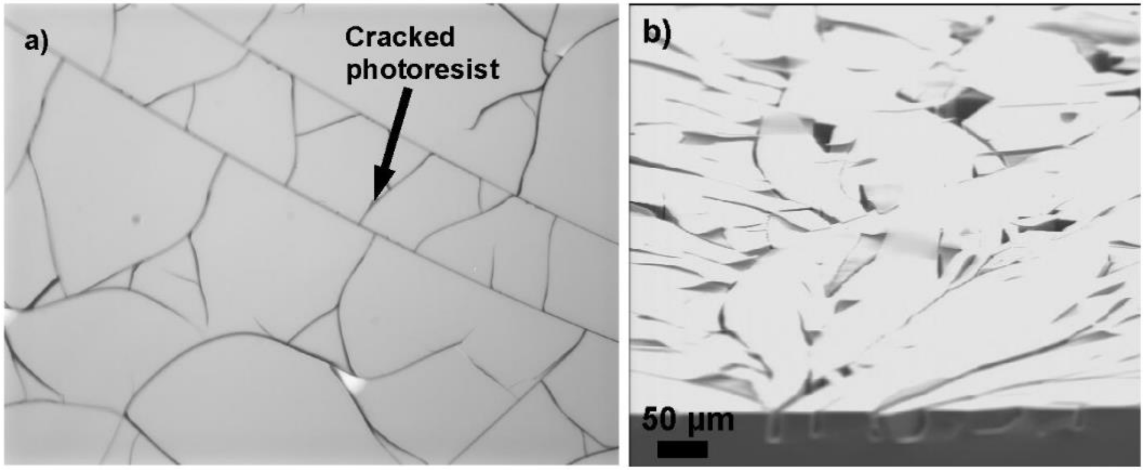
- However, MEMS devices, TSV and power devices manufacturing applications require extremely deep trenches where RIE process is not able to meet these requirements.

- DRIE allows to achieve high anisotropic etch profiles at high etch rates and with high aspect ratio structures required in MEMS devices, TSV and Power applications.

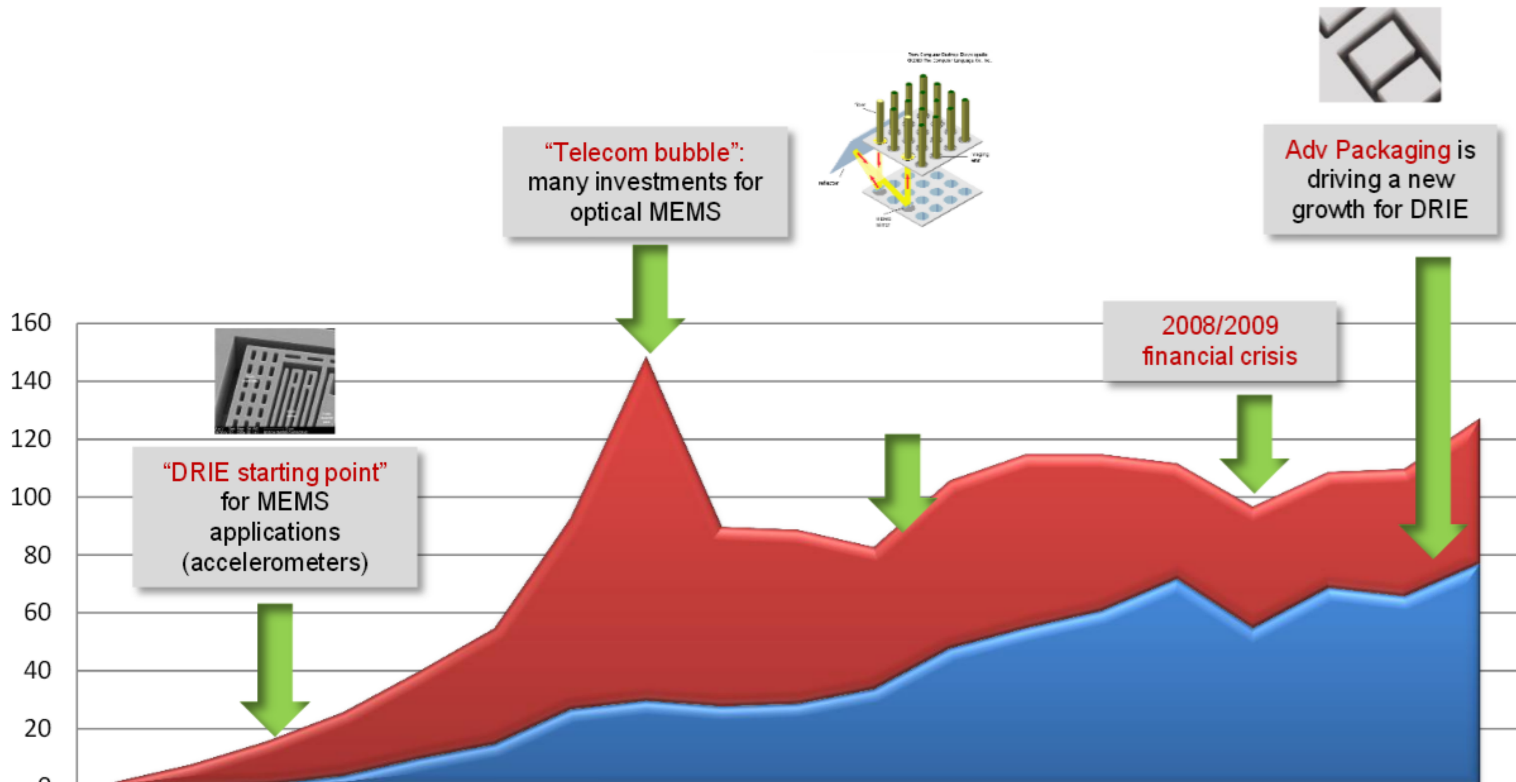


Source: Yole Development

In cryogenic-DRIE, the wafer is chilled to −110 °C (163 K). The low temperature slows down the chemical reaction that produces isotropic etching. However, ions continue to bombard upward-facing surfaces and etch them away. This process produces trenches with highly vertical sidewalls. The primary issues with cryo-DRIE is that the standard masks on substrates crack under the extreme cold, plus etch by-products have a tendency of depositing on the nearest cold surface, i.e. the substrate or electrode.



Sources: Yole Development
CRYOGENIC DEEP REACTIVE ION ETCHING OF SILICON MICRO AND NANOSTRUCTURES
Doctoral Dissertation, Helsinki University of Technology



	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
R&D / Production tools for MEMS	2	8	15	22	30	40	66	119	62	60	49	58	60	54	40	42	40	44	50
R&D / Production tools non-MEMS	0	0	1	4	10	15	27	30	28	29	34	48	55	61	72	55	69	66	77

Source: Yole Development

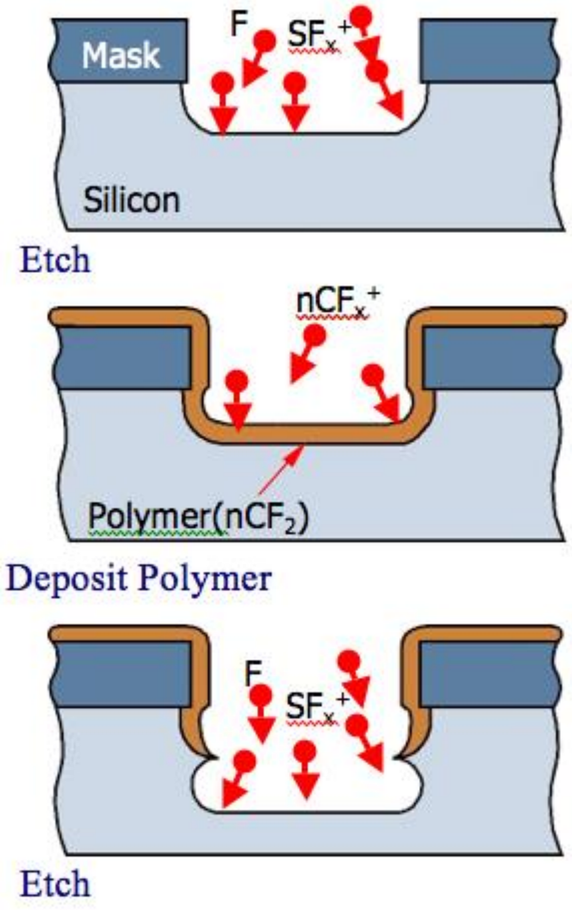
Two alternating steps with one process

1. Highly directional (vertical) etching by SF_x^+
2. Sidewall passivation with nCF_x^+

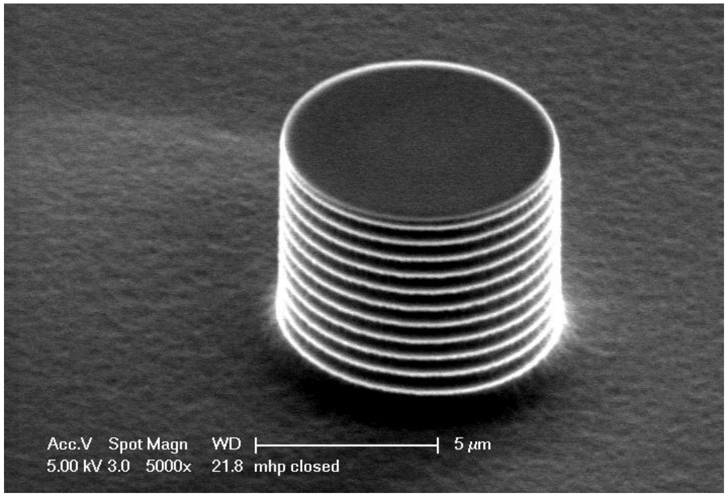
   (on the sides a polymer builds up that is not etched by the next etching sequence)

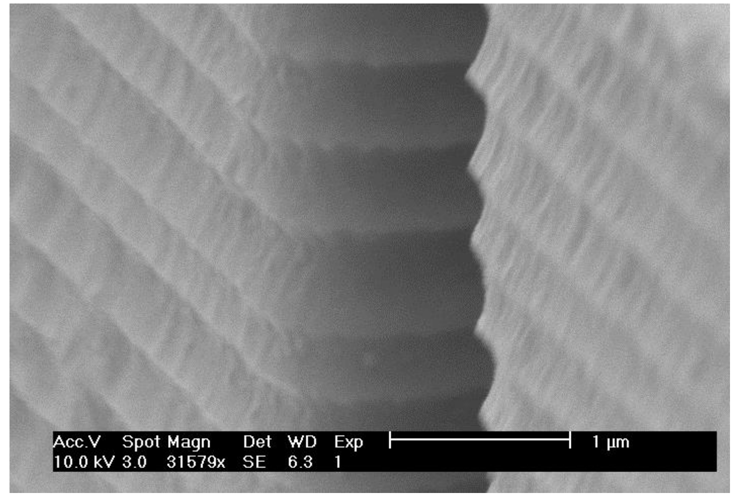
The passivation layer

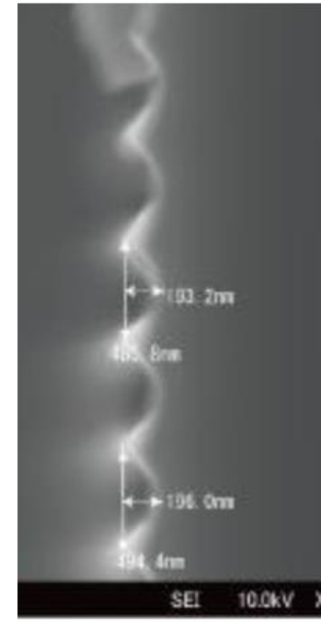
- A fluorine based polymer
- Removing by oxygen plasma or very strong etcher for organic materials (HNO_3 or "piranha" = mixture of H_2SO_4 and H_2O_2)



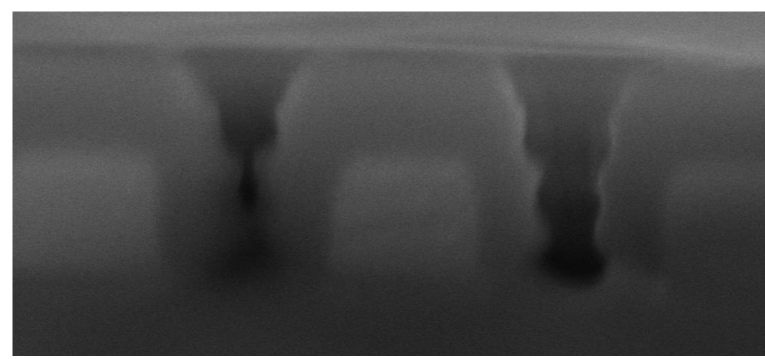
Scalloping effect



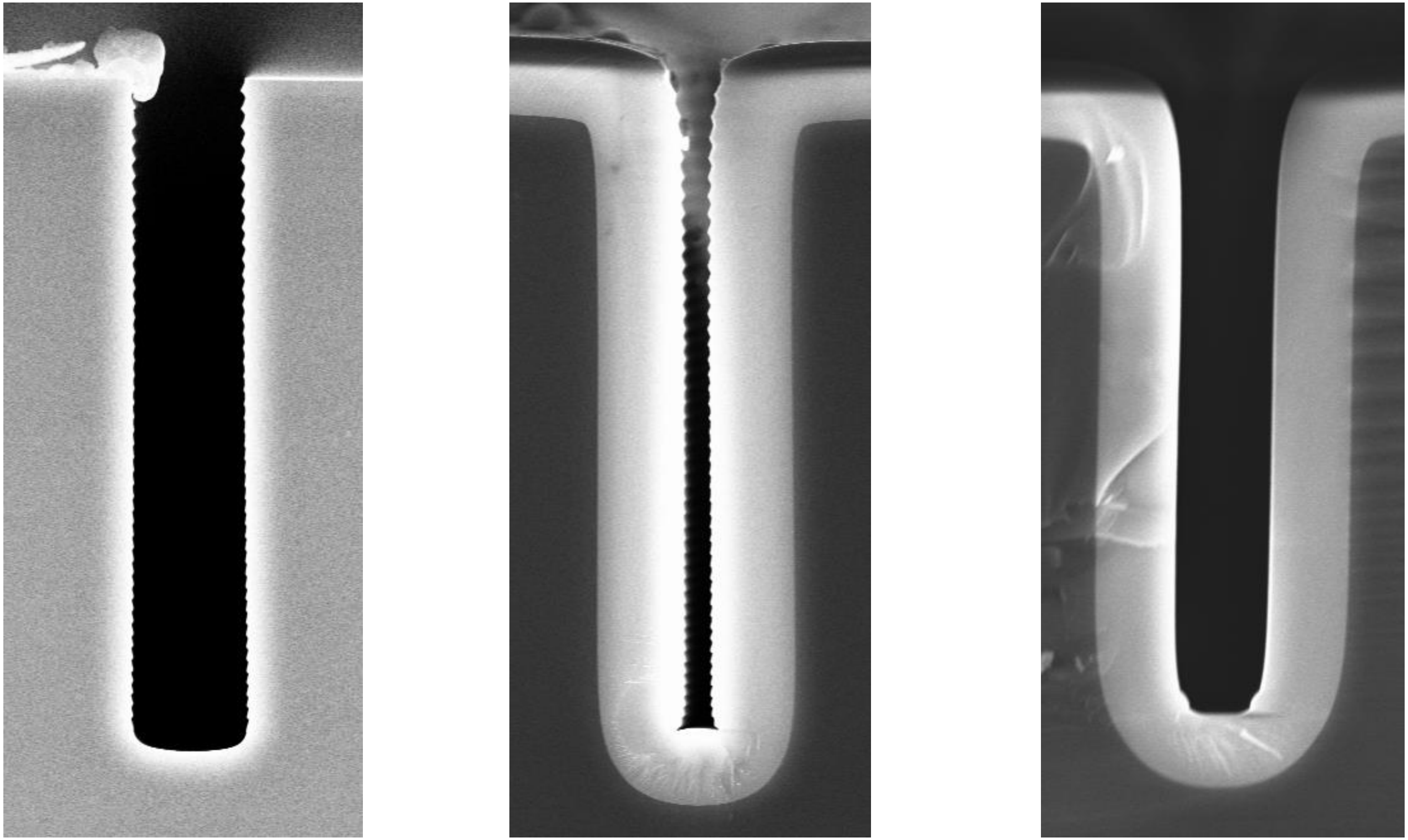




Scallop polishing by high temperature oxidation

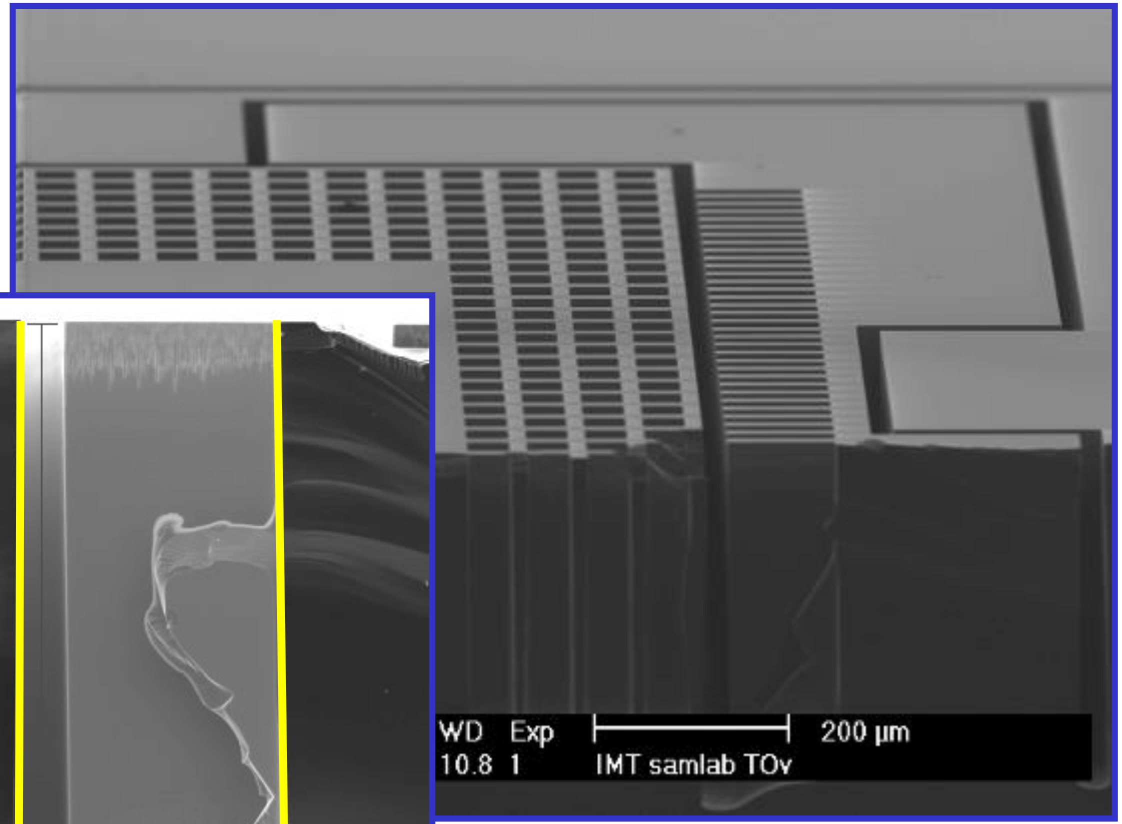


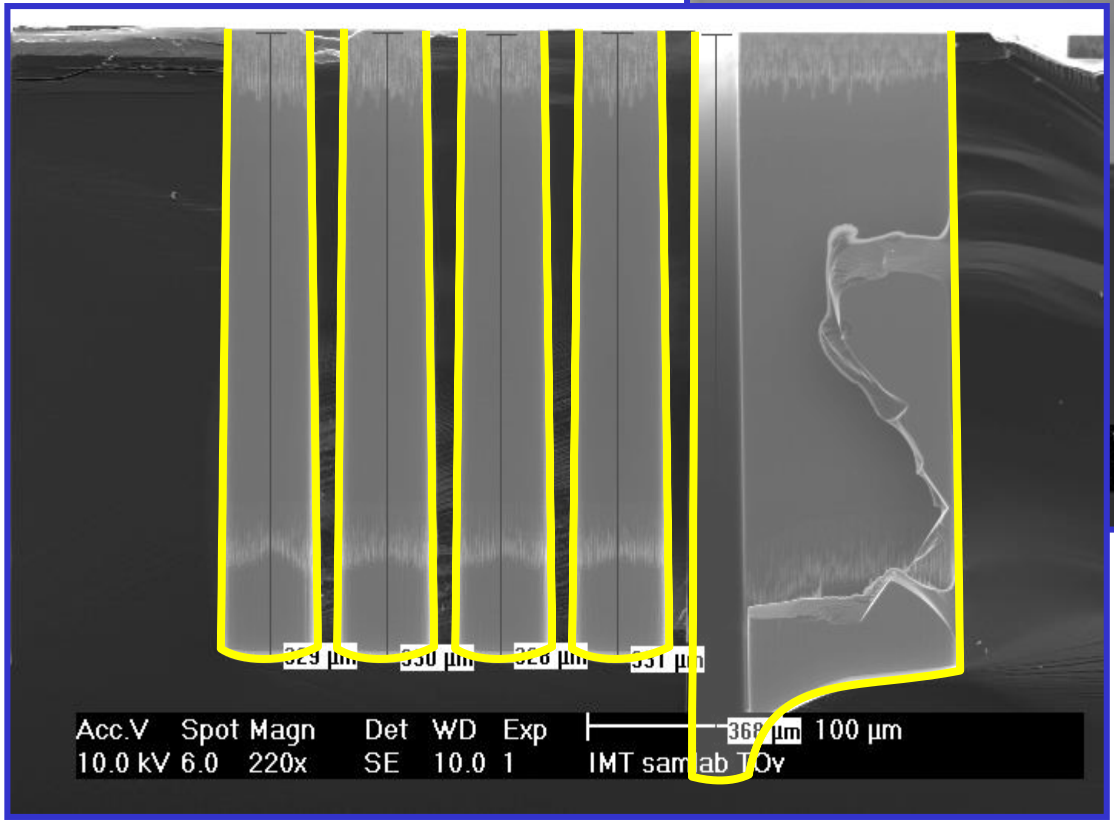
Scallop polishing by high temperature oxidation



Long trenches etch faster

→ Better exchange of etchants and products





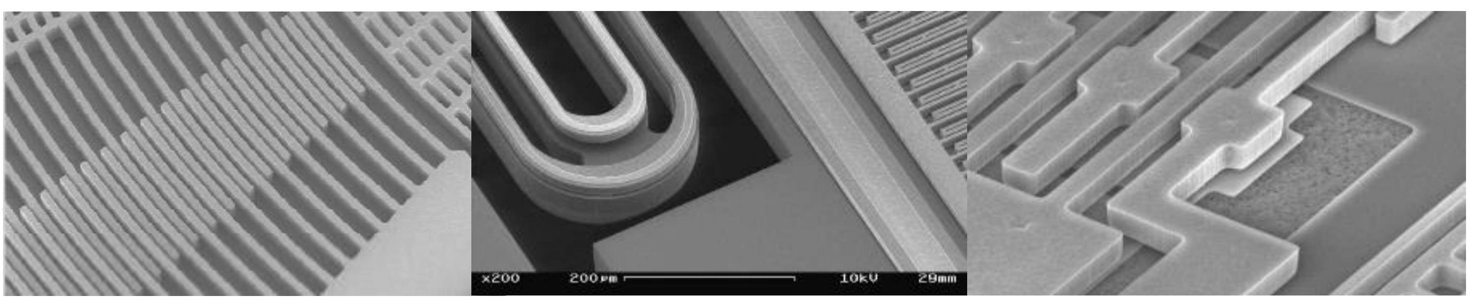
One of the MEMS Pioneers: Bosch

MEMS for Automotive and Consumer Applications

Bosch – the micromechanics pioneer

Bosch is a micromechanics pioneer with more than 20 years of experience

- First product in 1993: pressure sensor for automotive applications
- 1 billion MEMS sensors produced – 220 million units in 2009
- #1 in Automotive MEMS: Bosch
- More than 800 patents in the MEMS sensor field
- Creator of the “Bosch Process” (Deep Reactive Ion Etch - DRIE)
- “European inventor of the year” (2007) for the “Bosch process”



Automotive Electronics

BOSCH

Dr. Jiri Marek, Robert Bosch GmbH
“MEMS for Automotive and Consumer Applications”, IMS Chips 2010

Surface Micromachining: Thin Film Deposition techniques

- **Introduction to deposition techniques**
- **Physical vapor Deposition (PVD)**
    - Resistive thermal evaporation
    - Electron beam evaporation
    - Sputtering
- **Chemical vapor Deposition**
    - APCVD
    - PECVD
    - MOCVD
- **Oxidation methods**
    - Thermal oxidation
    - Annealing
- **Electrodeposition**
- **Epitaxy**
- **casting**

Introduction to deposition techniques

- **Depositions that happen because of a chemical reaction:**
  - Chemical Vapor Deposition (CVD)
  - Electrodeposition
  - Epitaxy
  - Thermal oxidation

These processes exploit the creation of solid materials directly from chemical reactions in gas and/or liquid compositions or with the substrate material. The solid material is usually not the only product formed by the reaction. Byproducts can include gases, liquids and even other solids.

- **Depositions that happen because of a physical reaction:**
  - Physical Vapor Deposition (PVD)
  - Casting

Common for all these processes are that the material deposited is physically moved on to the substrate. In other words, there is no chemical reaction which forms the material on the substrate. This is not completely correct for casting processes, though it is more convenient to think of them that way.

Physical vapor Deposition - vacuum

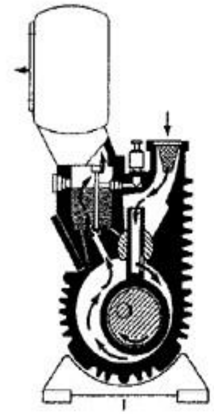
- The thin-film deposition techniques are closely related to the progresses made in the vacuum techniques (beginning WW II)
  - Example: (1935: Al mirror coating, Palomar telescope)

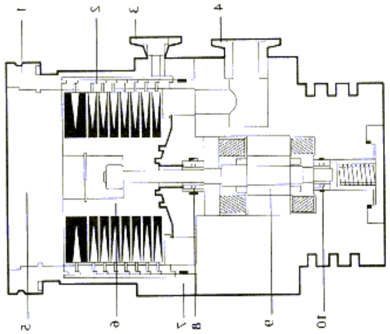
- Classification of the vacuum:
  - Forvacuum (technical) $p > 10^{-3}$ Torr (1 mbar = 0.75 Torr)
  - Low vacuum (LV) $10^{-3} > p > 10^{-6}$
  - High vacuum (HV) $10^{-6} > p > 10^{-9}$
  - Ultra high vacuum (UHV) $10^{-9} > p > 10^{-12}$
  - Extremely high vacuum $p < 10^{-12}$ (ex: space vacuum)

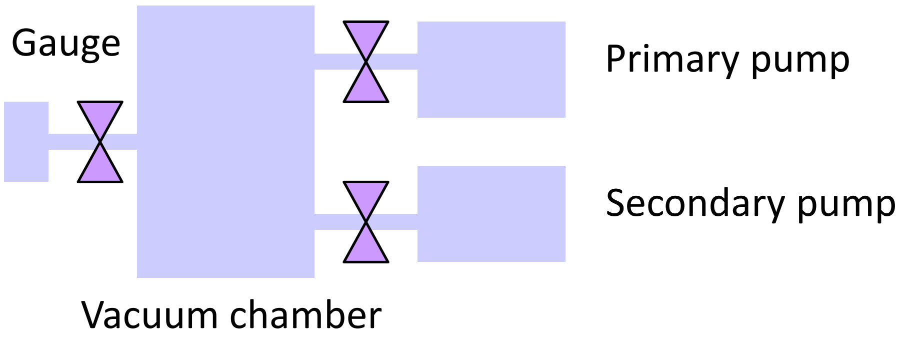
- The PVD process needs a high vacuum (for medium quality) and UHV (for higher film quality)
  - Avoid contamination, O_2, …
  - Allow a better homogeneity of the deposited layer

Physical vapor Deposition - vacuum

- Vacuum system:
  - Vacuum chamber with valves and gauges
  - Primary pump:
    - rotatory pump, …
    - Range: atmospheric to 10^{-3} Torr
  - Secondary pump:
    - turbomolecular pumps (24’000 - 36’000 rpm)
    - Range: 10^{-3} to 10^{-10} Torr



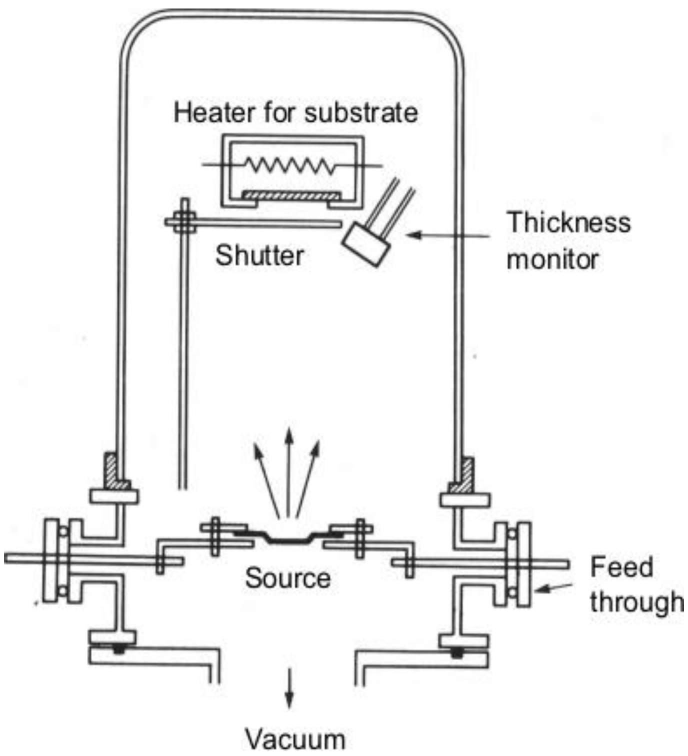




PVD: resistive thermal evaporation

- Principle: electrically heated filament or crucible
- Resistive evaporation system requirements
  - Vacuum system (pumps, chamber, valves…)
  - Thickness monitor
  - Mechanical shutter:

    Evaporation rate is set by temperature of source, but this cannot be turned on and off rapidly. A mechanical shutter allows evaporant flux to be rapidly modulated.
  - Electrical power:
    - Either high current or high voltage



PVD: resistive thermal evaporation, sources

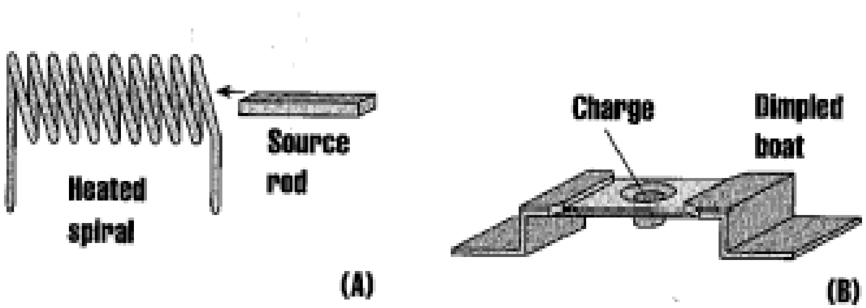
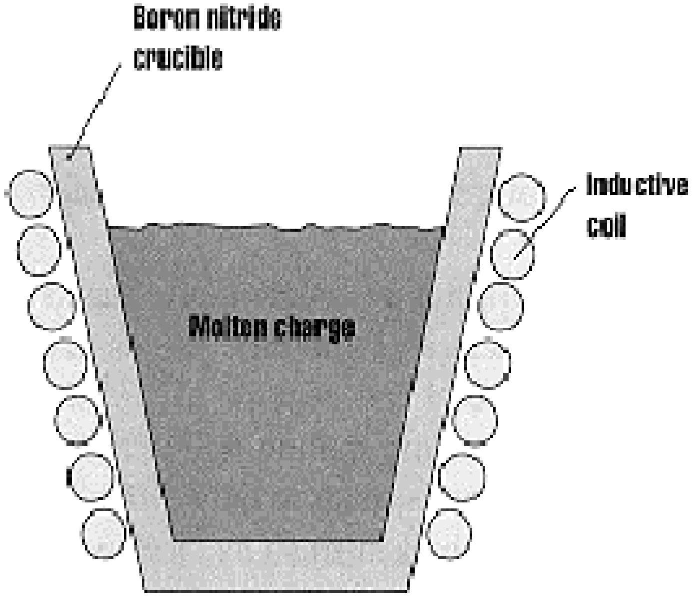
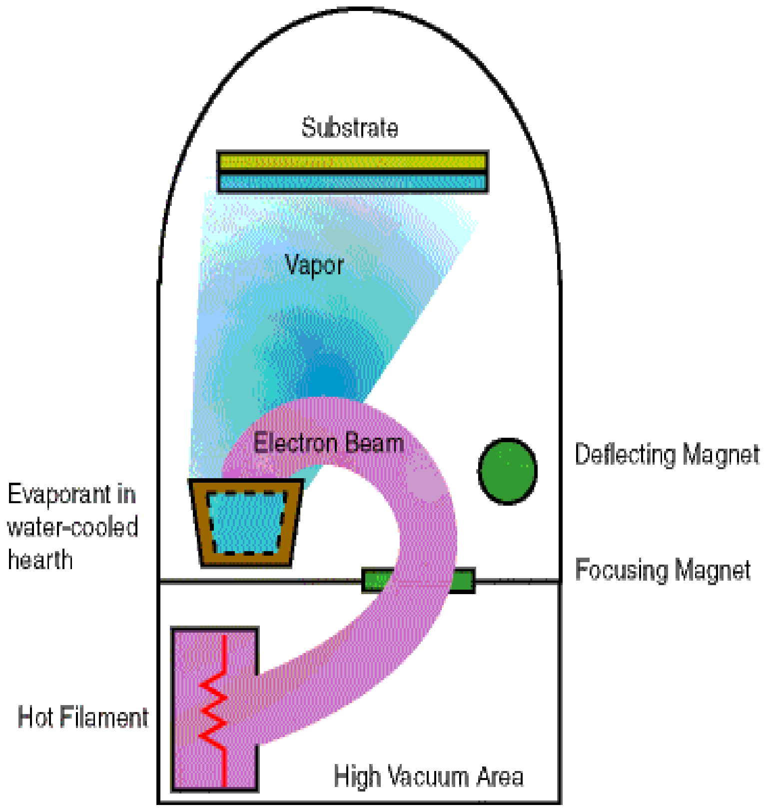


Figure 12-6 Resistive evaporator sources. (a) Simple



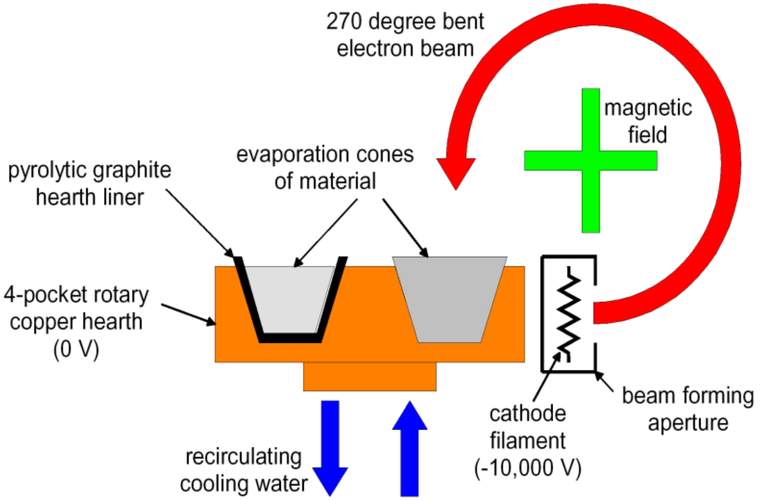
PVD: Electron Beam thermal evaporation

- Principle: electron-beam evaporation, scan of the EB on the crucible
- EB evaporation system requirements
  - Vacuum system (pumps, chamber, valves…)
  - Magnet for beam deflection
  - Cooling system
  - Thickness monitor
  - Mechanical shutter:
    - Evaporation rate is set by the energy of the e-beam. A mechanical shutter stopps the evaporant flux during the first seconds that follow the switching on of the e-beam.
  - Electrical power:
    - Energy of the source: 10 kV



PVD: Electron Beam thermal evaporation

- 270° bent beam electron gun is most preferred:
  - Filament is out of direct exposure from evaporant flux.
  - Magnetic field can be used for beam focusing.
  - Magnetic field can be used for beam positioning.
  - Additional lateral magnetic field can be used produce X-Y sweep.

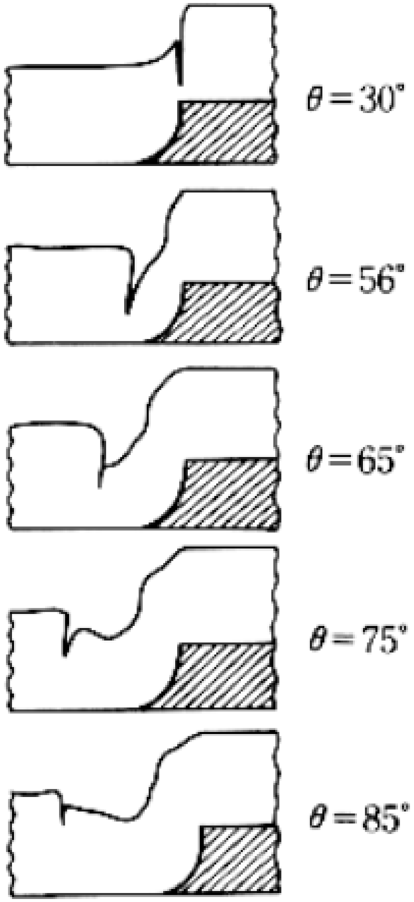


Photograph of a deflected e-beam

PVD: EB thermal evaporation, characteristics

- Evaporant melt locally, no contact with the crucible => low contamination
- More complex, but extremely versatile.
- Can achieve temperatures in excess of 3000°C.
- Typical deposition rates are 10-100 Angstroms/second.
- Common evaporant materials:
  - Everything a resistance heated evaporator will accommodate
  - Pt, Au, Ir, Ni, Rh, Ti, V, Zr, W (3410°C), Ta(3300°C),
  - Mo (2620°C)
  - Al_2O_3 (2030°C), SiO, SiO_2, SnO_2, TiO_2, ZrO_2
- Exposes substrate to secondary electron radiation.
  - X-rays can also be generated by high voltage electron beam.
- Alloys difficult to deposit

PVD: thermal evaporation, step coverage



In order to have a good step coverage, a planetary system can be used.

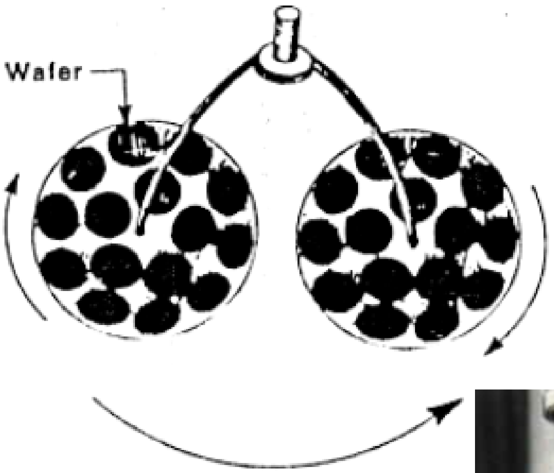
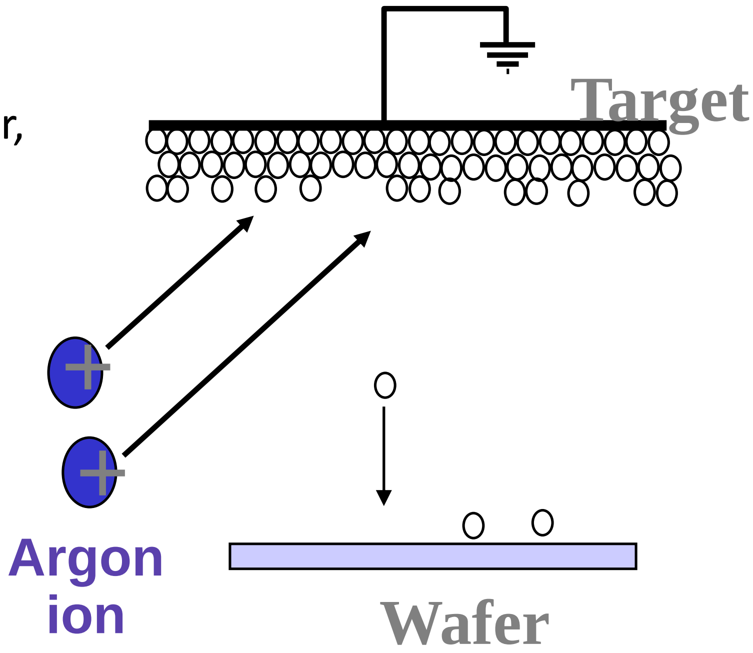


Fig. 16.10
Planetary Wafer Holder

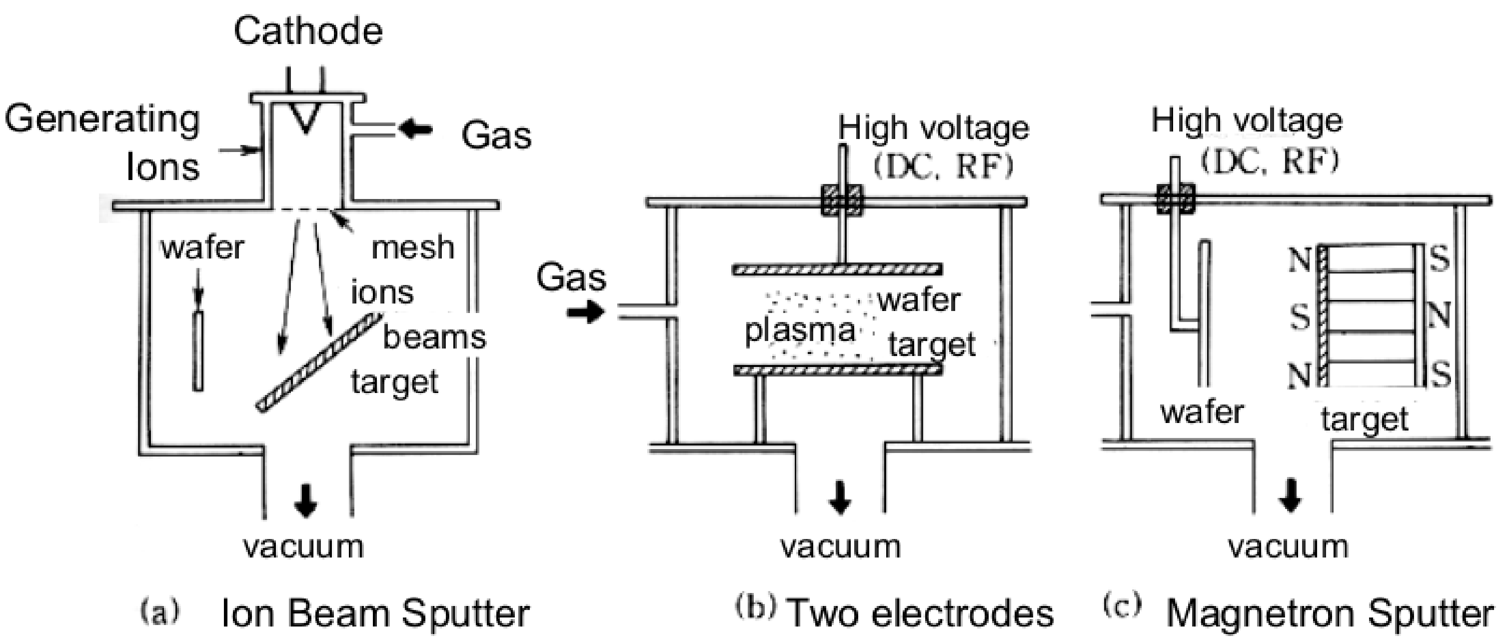
PVD: sputtering, description

- Principle: Sputtering is a physical phenomenon involving the acceleration of ions, usually Ar+, through a potential gradient, and the bombardment by these ions of a "target" or cathode. Through momentum transfer, atoms near the surface of the target material become volatile and are transported as a vapor to the substrate. At the substrate, the film grows through deposition.

- Sputtering system requirements
  - Vacuum system (pumps, chamber, valves…)
  - Target for each metal or alloys
  - Cooling system
  - Thickness monitor
  - Electrical power: DC or RF power supply

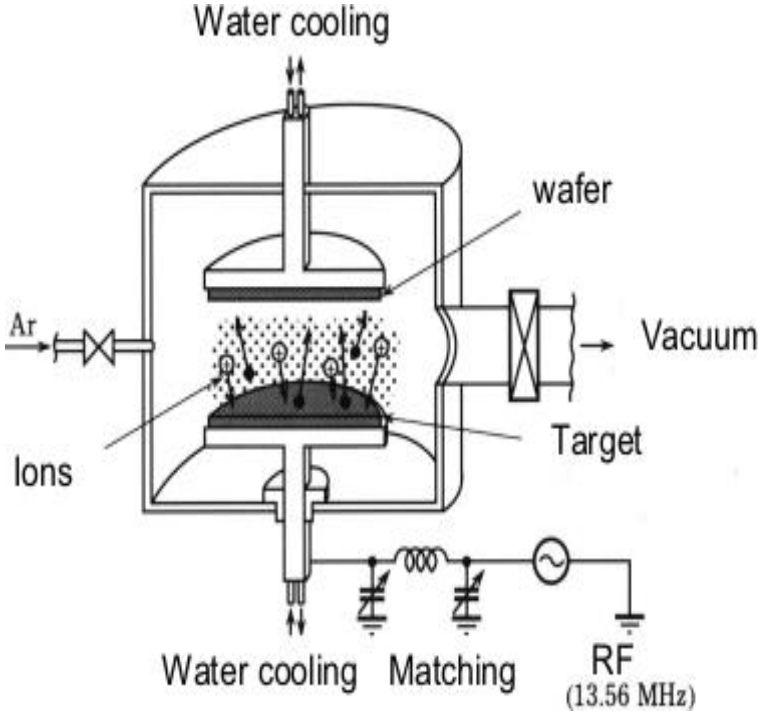


PVD: sputtering, different methods



PVD: sputtering, description

- Some characteristics of sputter deposition are:
  - The ability to deposit alloy films with composition similar to that of the target
  - Better step coverage than evaporation deposition (planar target)
  - Adhesion is improved



PVD: Evaporation vs. Sputtering

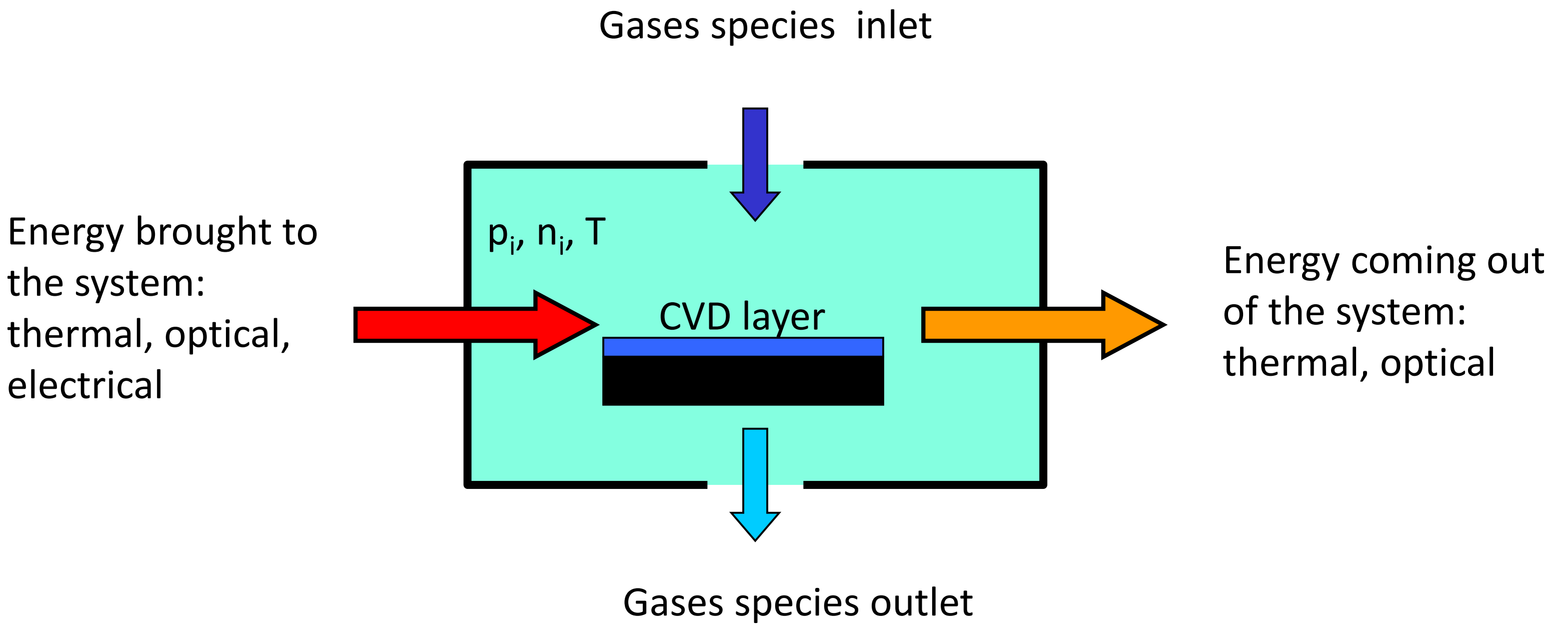
	Evaporation	Sputtering
Growth rate	thousand of atomic layer/s	one atomic layer/s
	ex: 0.5 μm/min Al	
Choice of material	Limited	Almost unlimited
Purity	Excellent (HV to UHV)	Medium (LV to HV)
Substrate heating	very low	substantial
Substrate damage	very low	ionic bombardement damage
In-situ cleaning	not an option	easily done
Alloy composition, stochiometry	Little or no control	Alloy composition can be tightly controlled
X-ray damage	only with e-beam evaporation	Radiation and particle damage possible
Source material	Medium	Expensive
Uniformity	Difficult	Easy over large areas
Equipment	Low cost	More expensive
Adhesion	Often poor	Excellent
Film properties		
(e.g.grain size, step coverage)	Difficult to control	Controlled by bias, pressure, substrate heat

Chemical Vapour Deposition processes

Process of chemically reacting a volatile compound to be deposited with other gases to produce a nonvolatile solid that deposits on a substrate

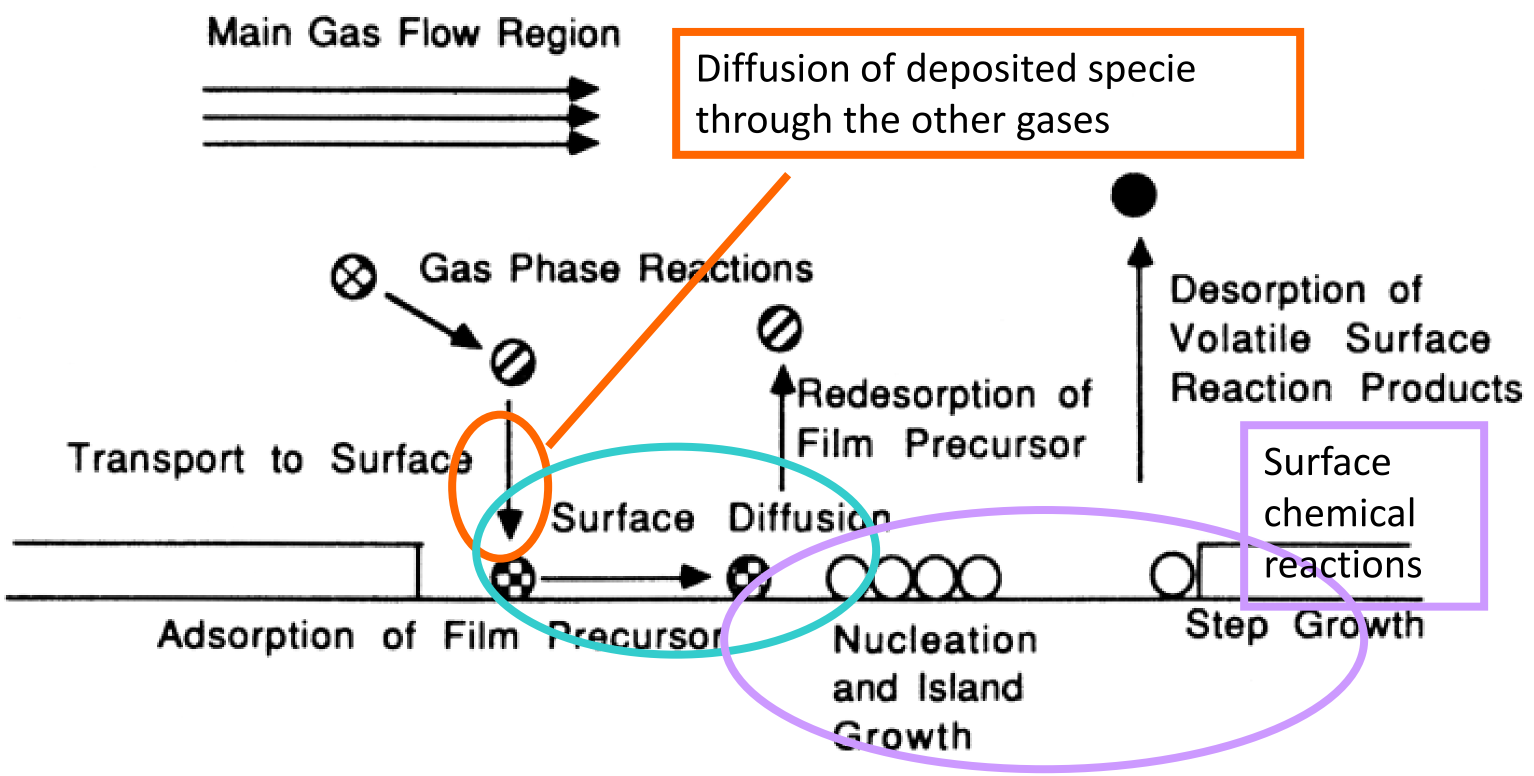
M.Ohring, « The Materials Science of Thin Films », Academic Press INC, 1992.

CVD principle



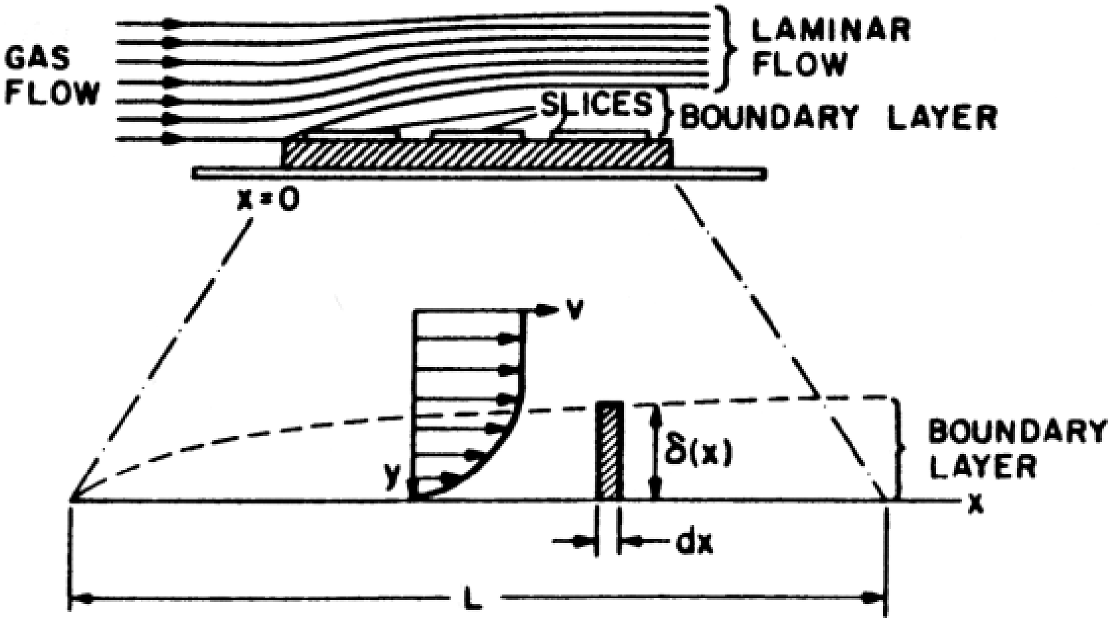
The energy transfer and gas flow have to be optimized in order to ensure an homogenous deposition at the surface of the wafer. The state of the gases (p_i, n_i, T) has also a major influence on the deposition.

CVD Deposition process



The precursors cross the boudary layer by diffusing through the other gases species. The deposition rate can be limited by: the crossing of the boudary layer, physical phenomenon such as absorbtion diffusion on the surface, or chemical reactions on the surface. The slowest of the process dominates the raction.

Boundary layer



$$\delta(x) = \left(\frac{\eta x}{\rho U}\right)^{1/2}$$

$$\langle\delta\rangle_L = \frac{2}{3}\left(\frac{\eta L}{\rho U}\right)^{1/2}$$

$$\langle\delta\rangle_L = \frac{2}{3}\left(\frac{\eta L T}{p M U}\right)^{1/2}$$

Layer close to a solid surface where the gas speed is lower than in the rest of the gas flow section. In the boudary layer, the speed flow gradient is different to zero.

Flux in the boundery layer

Some species are absorbed by the surface and therefore diffuse through the boundery layer.
Flux of the deposited material in the boundary layer due to diffusion:

$$\phi = D\frac{dc}{dx}$$

$$\langle\phi\rangle_L = D\frac{\Delta c}{\langle\delta\rangle_L} = \frac{3D\Delta c}{2}\left(\frac{\rho U}{\eta L}\right)^{1/2}$$

$$\langle\phi\rangle_L = \frac{3D\Delta c}{2}\left(\frac{pMU}{\eta LT}\right)^{1/2}$$

Parameters influence:

$$\phi \propto \sqrt{U}$$

$$\phi \propto \sqrt{pressure}, T = cte$$

$$\phi \propto D \propto T^{1.75to2} \Rightarrow \phi \propto T^{1.25to1.5}$$

$$\Delta c = cte(t) \Rightarrow absorbtion = cte(t)$$

c: concentration of the deposited material

D: diffusion coefficient of the deposited material in the other gases

U: gas stream velocity

r: gases average density

h: gases average viscosity

L: plate length

Surface physical phenomon

The growing speed can be modelled by a thermally activated phenomon:

$$R = R_0 e^{-E_a / kT}$$

R: growing speed (frequency factor)

E_a: activation energy

k: Boltzmann constant

The highee the temperature, the faster the reaction!

Surface chemical reactions

The speed of the film formation, when limited by surface chemical reactions, is mainly dependant on the partial pressure of the gas specie deposited and its molair mass.

$$\frac{1}{\Gamma} = \frac{1}{\alpha p_i} + \frac{\beta}{\alpha}$$

G: film deposition speed

p_i: partial pressure

a, b: coefficients molair mass dependant

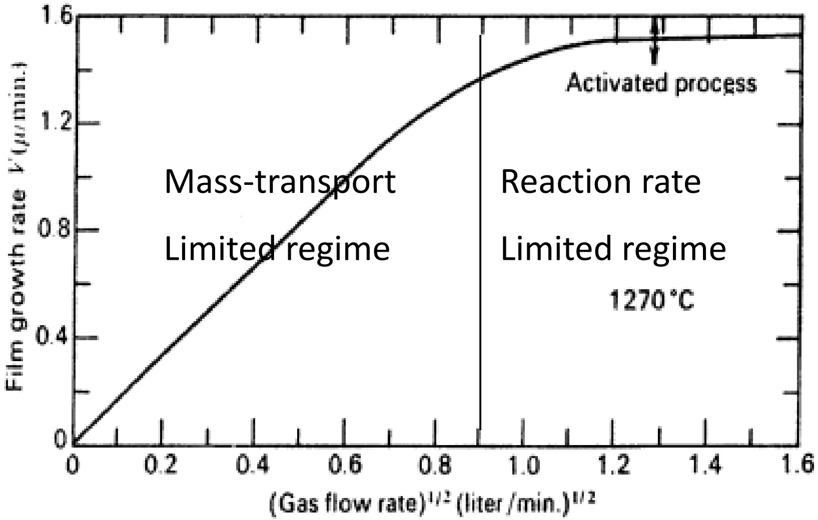
Deposition speed

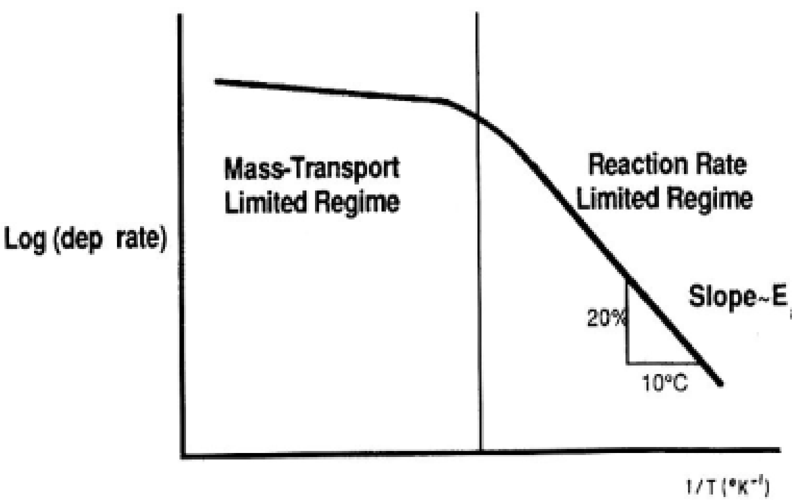
In the case of a deposition speed limited by one of these two reasons (no speed limitations due to chemical reactions):

a) crossing of the boudary layer

b) physical surface phenomenons

The following graphs show the deposition speed when the limitation is varied from type a) to b).



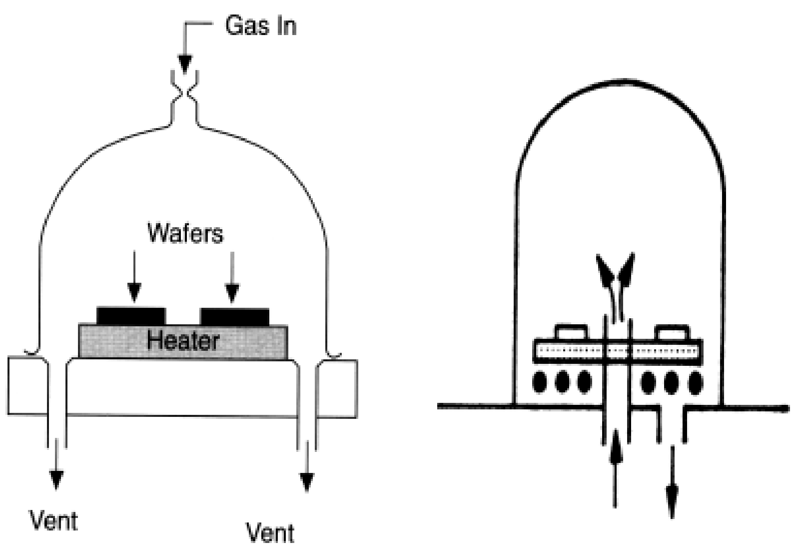


CVD Deposition methods

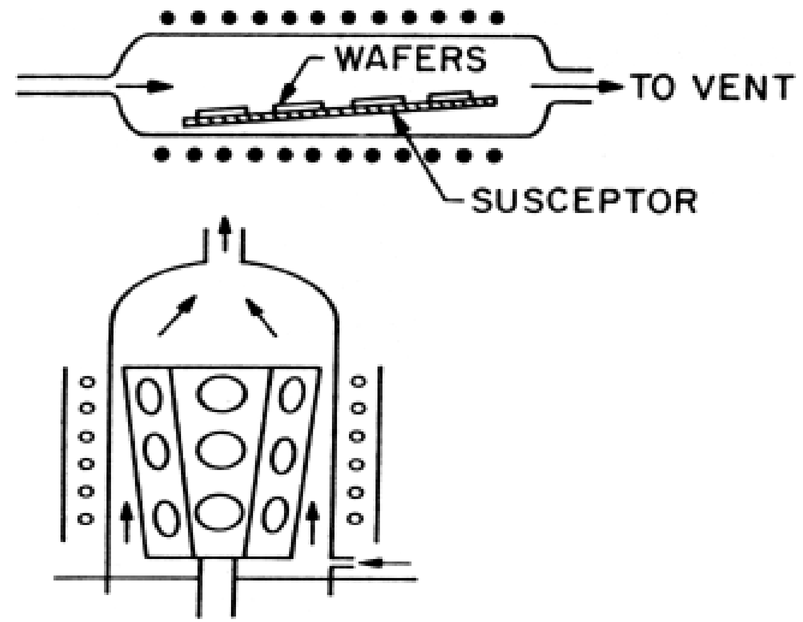
- APCVD: Atmospheric Pressure Chemical Vapor Deposition
- PECVD: Plasma-Enhanced Chemical Vapor Deposition
- LPCVD: Low-Presure Chemical Vapor Deposition
- MOCVD: MetalOrganic Chemical Vapor Deposition (LPCVD)
- LECVD: Laser-Enhanced Chemical Vapor Deposition
- VLPCVD: Very Low Pressure Chemical Vapor Deposition

APCVD reactors

Cold wall



Hot wall



Pressure: ~atmospheric, 10 to 100 kPa

Deposition temperature: (350-900) °C

Mass-transport controlled

Applications: oxides

High deposition rate: SiO_2, 670 A/min

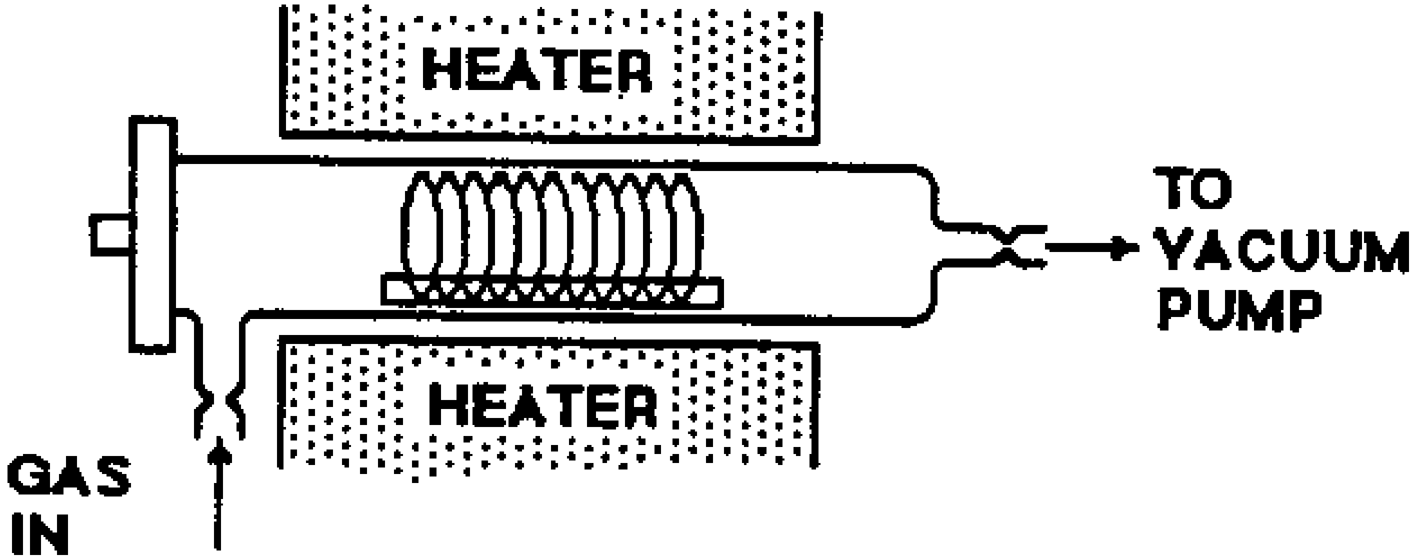
Poor step coverage

APCVD



Layers available: Al_2O_3, SiO_2 (doped or undoped)

LPCVD reactor



Pressure: 10-100 Pa

Deposition temperature: 550-600 °C

Surface reaction controlled

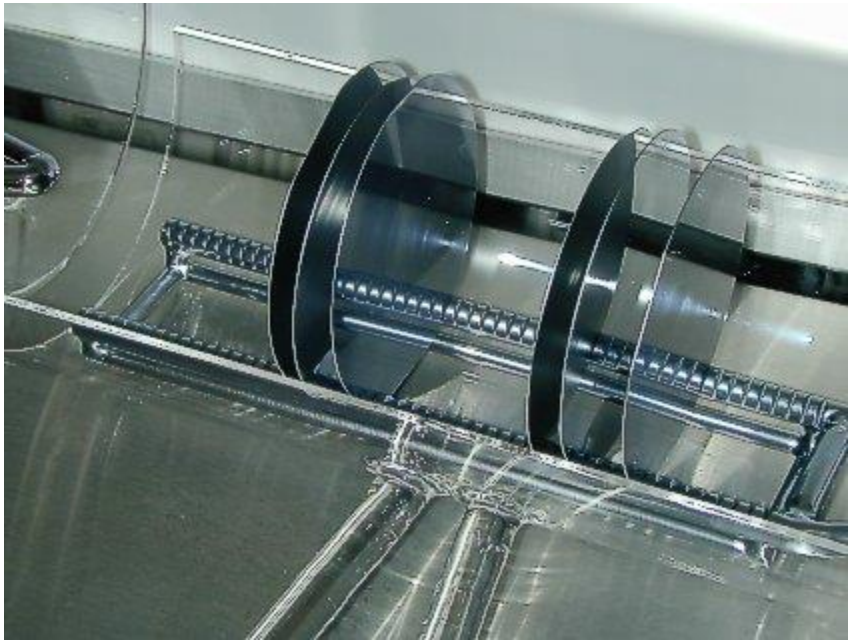
Applications: oxides, nitrides, poly-Si

Low deposition rate: Si_3N_4, 50 A/min

Comformable step coverage

Excellent uniformity and purity

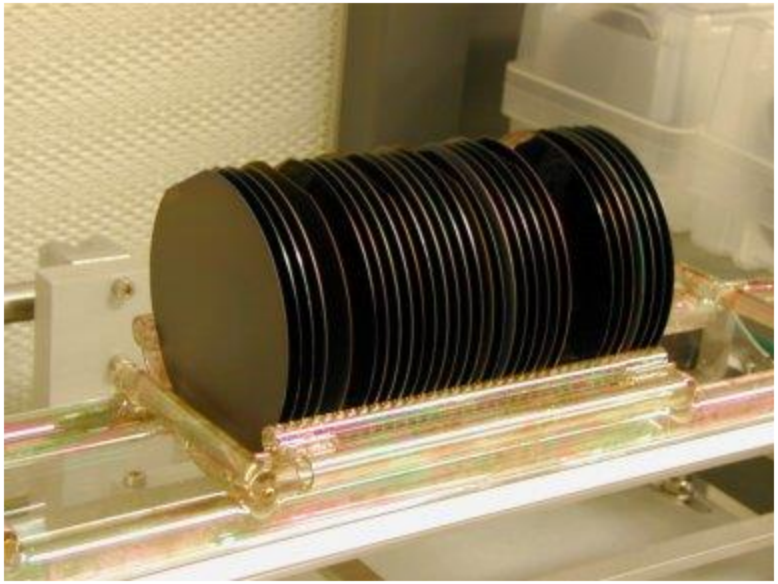
LPCVD



Layers available: Si_3N_4, poly-Si

MOCVD

Reactor similar to LPCVD reactor



Pressure: 10-100 Pa

Deposition temperature: 450 °C

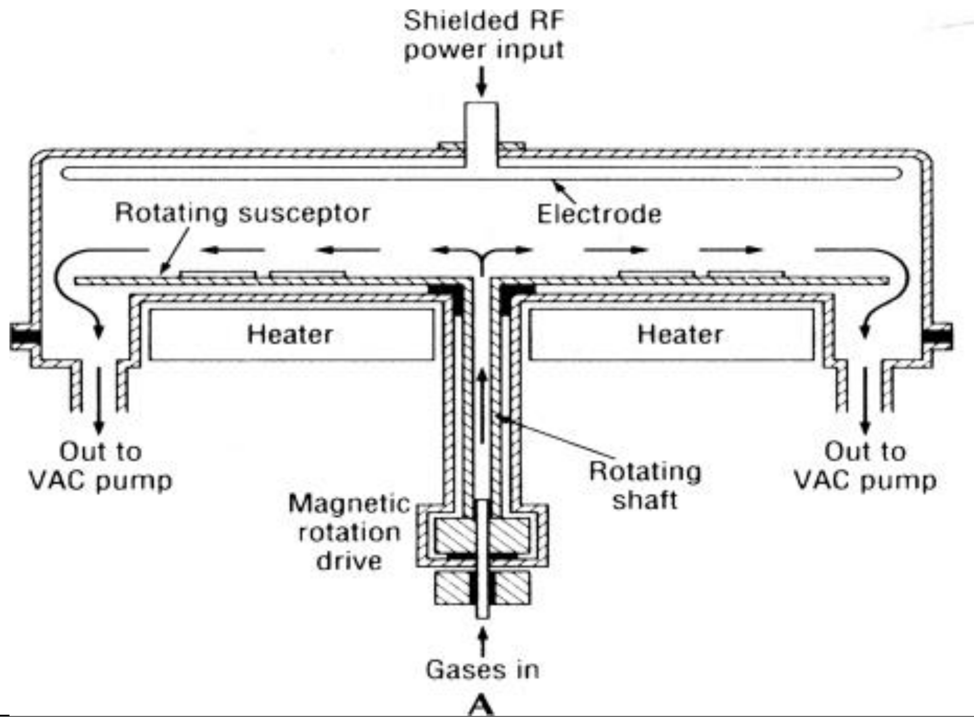
Surface reaction controlled

Layer available: Ta_2O_5

Low deposition rate: Ta_2O_5, 20-60 A/min

Excellent for epitaxial layers

PECVD reactors



Pressure: 250-1000 Pa

Deposition temperature: 300-400 °C

Applications: nitrides and oxides

Low deposition rate: Si_3N_4, 50 A/min

Good step coverage, few pinholes

Hydrogen contamination

PECVD

Layers available: Si_3N_4, SiO_2

Some CVD layers properties

	Si_3N_4, PECVD	Si_3N_4, LPCVD	SiO_2, APCVD	Poly-Si, LPCVD
T [°C]	400	750	400	650
Step coverage	good	comformable	poor	comformable
Density [kg/m^{3}]	2400-2800	2900-3100	2100	2330
Stress [MPa]	200 comp-500 tens	0-1 tensile	300 tensile	20-30 tensile
Diel.strength [kV/mm]	0.5	1	0.8	
Resistivity [Wcm]	10^6-10^{15}	10^{16}		

References

[1] Semiconductor Material and process technology handbook
Gary Mc Guire

[2] VLSI Technology
S.M. Sze

[3] The materials science of thin film
Milton Ohring

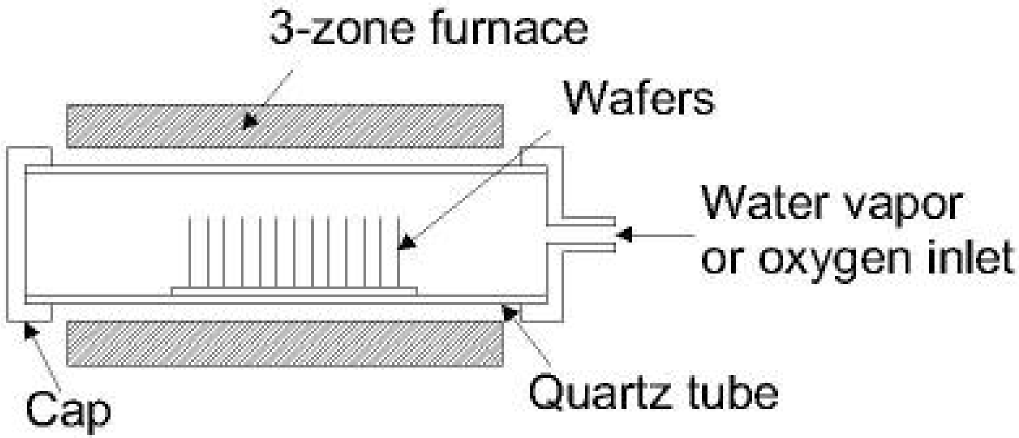
[4] Handbook of thin film technology
Maissel and Glanz

[5] Semiconductor devices Physics and Technology
S.M. Sze

[6] Electronic Materials Science and Technology
S. Murarka

Thermal oxidation

his is one of the most basic deposition technologies. It is simply oxidation of the substrate surface in an oxygen rich atmosphere. The temperature is raised to 800° C-1100° C to speed up the process. This is also the only deposition technology which actually consumes some of the substrate as it proceeds. The growth of the film is spurned by diffusion of oxygen into the substrate, which means the film growth is actually downwards into the substrate.



Thermal oxidation

SiO_2 growth is a key process step in manufacturing all Si devices.

- Thick oxides (>5000 Å) are used for field oxides to isolate devices from one to the other
- Thin gate oxides (<1000 Å) to control MOS devices
- Sacrificial layer are grown as mask and removed

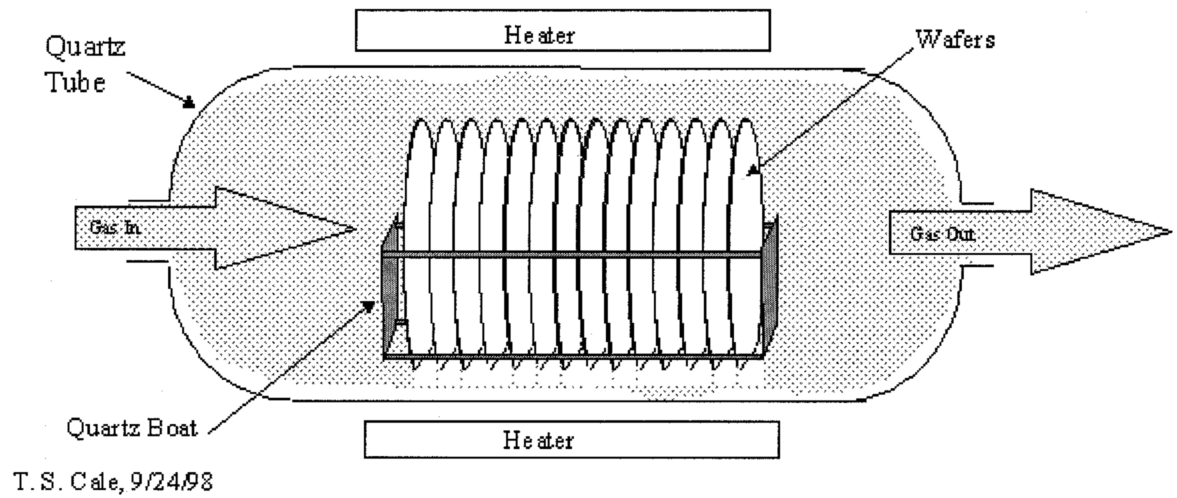
The stability and ease of formation of SiO_2 was one of the reason that Si replaced Ge

Thermal oxidation

Wafers are heated in an atmosphere containing an oxidant, usually, O_2, steam, or N_2O.

- Dry oxidation $Si + O_2 \rightarrow SiO_2$

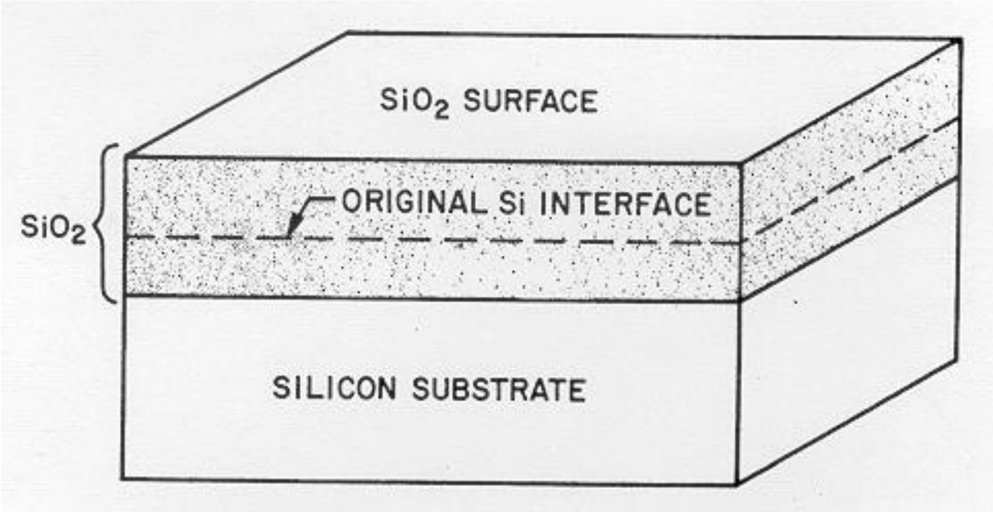
- Wet oxidation $Si+2H_2O \rightarrow SiO_2+2H_2$



Thermal oxidation

Kinetics of growth

The Si-SiO_2 interface moves into the Si during the oxidation. This creates a fresh region of Si-SiO_2



Thermal oxidation

If a SiO_2 layer of thickness x is grown from thermal oxidation, what is the thickness of Si being consumed.

$$\frac{\text{Molecular weight of Si}}{\text{Density of Si}} = \frac{28.09 \ \text{g/mole}}{2.33 \ \text{g/cm}^3} = 12.06 \ \text{cm}^3/\text{mole}\,.$$

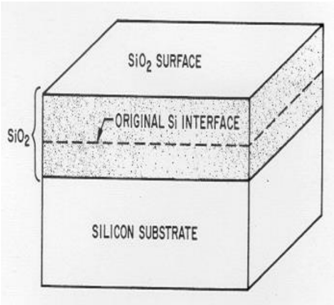
The volume of 1 mole silicon dioxide is

$$\frac{\text{Molecular weight of SiO}_2}{\text{Density of SiO}_2} = \frac{60.08 \ \text{g/mole}}{2.21 \ \text{g/cm}^3} = 27.18 \ \text{cm}^3/\text{mole}\,.$$

Since 1 mole silicon is converted to 1 mole silicon dioxide,

$$\frac{\text{Thickness of Si} \times \text{area}}{\text{Thickness of SiO}_2 \times \text{area}} = \frac{\text{volume of 1 mole of Si}}{\text{volume of 1 mole of SiO}_2}$$

$$\frac{\text{Thickness of Si}}{\text{Thickness of SiO}_2} = \frac{12.06}{27.18} = 0.44$$



That is to grow 1000 Å of SiO_2, a layer of 440 Å of Si is consumed.

Thermal oxidation

Basic structural unit of thermally grown SiO_2

- **SiO_2 surrounded tetrahedraly by four oxygen ions.**
- **When Si is thermally oxidized, the SiO_2 structure is amorphous.**

Density:

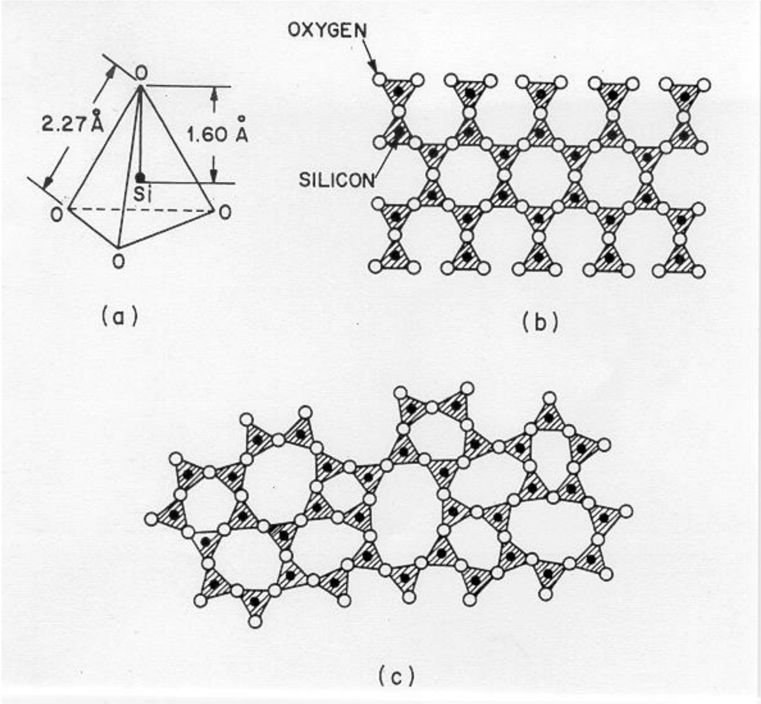
amorphous=2.21 g/cm^3,

quartz=2.65 g/cm^3.

(a) Basic unit of SiO_2

(b) quartz crystal

(c) amorphous



Thermal oxidation

Deal-Grove model

$$F_1 = D \cdot \frac{dC}{dx} \cong \frac{D \cdot (C_0 - C_s)}{x}$$

$$F_2 = k \cdot C_s$$

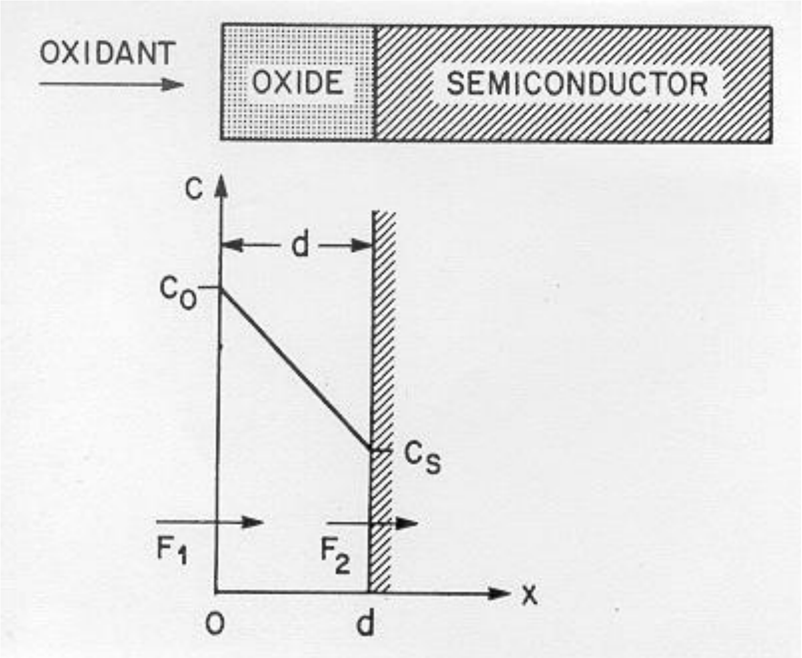
F1,F2: flux

D: diffusion coefficient

C_o,C_s : concentration of oxidant

x: thickness of the actuel SiO_2

k: surface reaction rate



At the steady state,

F_1=F_2=F

Thermal oxidation

At the steady state (elimination of $C_s = F_2/k = F/k$)

$$\frac{dx}{dt} = \frac{F}{C_1} = \frac{D \cdot C_o / C_1}{x + (D/k)}$$

C1: number of molecules to be oxidized

The solution of this differential equation is

$$x^2 + A \cdot x = B \cdot (t + \tau)$$

A=2D/k,

B=2DC0/C1,

B/A=KC0/C1

t= $(d_0^2 + 2Dd_0/k)C_1/2DC_0$

d_0: initial oxide layer

Thermal oxidation

linear $t \ll A^2/4B$ parabolic $t \gg A^2/4B$

$$x = \frac{B}{A}(t+\tau)$$

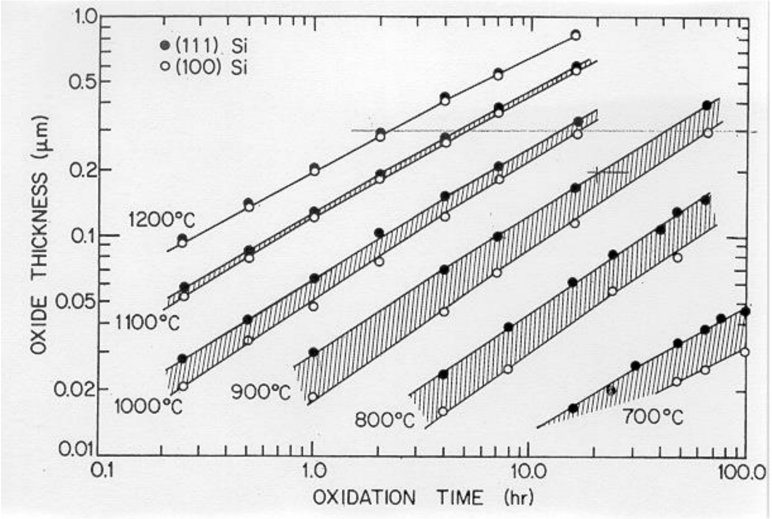
$$x^2 = B\cdot(t+\tau)$$

Oxidation temperature (°C)	Orientation	A (μm)	Parabolic rate constant B (μm²/h)	Linear rate constant B/A (μm/h)
900	(100)	0.95	0.143	0.150
	(111)	0.60	0.151	0.252
950	(100)	0.74	0.231	0.311
	(111)	0.44	0.231	0.524
1000	(100)	0.48	0.314	0.664
	(111)	0.27	0.314	1.163
1050	(100)	0.295	0.413	1.400
	(111)	0.18	0.415	2.307
1100	(100)	0.175	0.521	2.977
	(111)	0.105	0.517	4.926

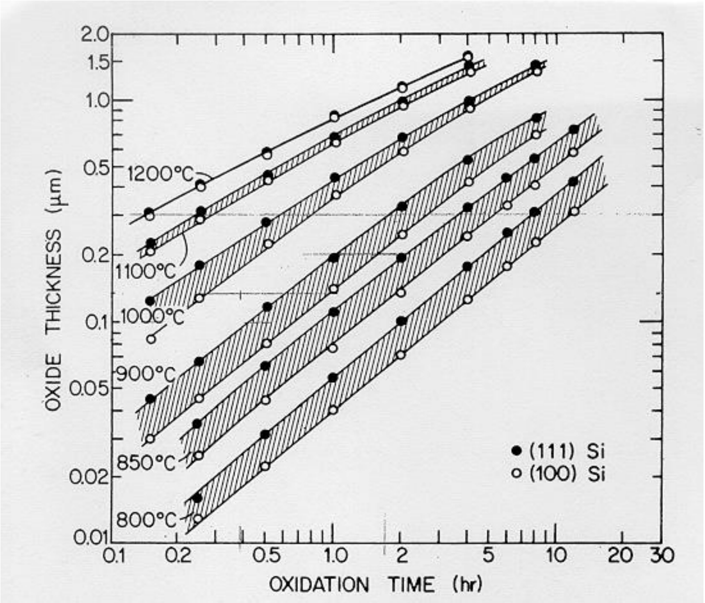
Table 1 Deal-grove, Rate constants for dry oxidation of Si

Thermal oxidation

Experimental results of SiO_2 thickness as a function of reaction time and temperature.



a) Dry oxidation growth



b) Steam growth

Thermal oxidation

Deal-grove: Summary

$$x^2 + A \cdot x = B \cdot (t + \tau)$$

Dry oxidation

Model fits well for growth of SiO_2 > 300 Å.

Wet oxidation

Model fits fairly well for growth of all SiO_2 thicknesses.

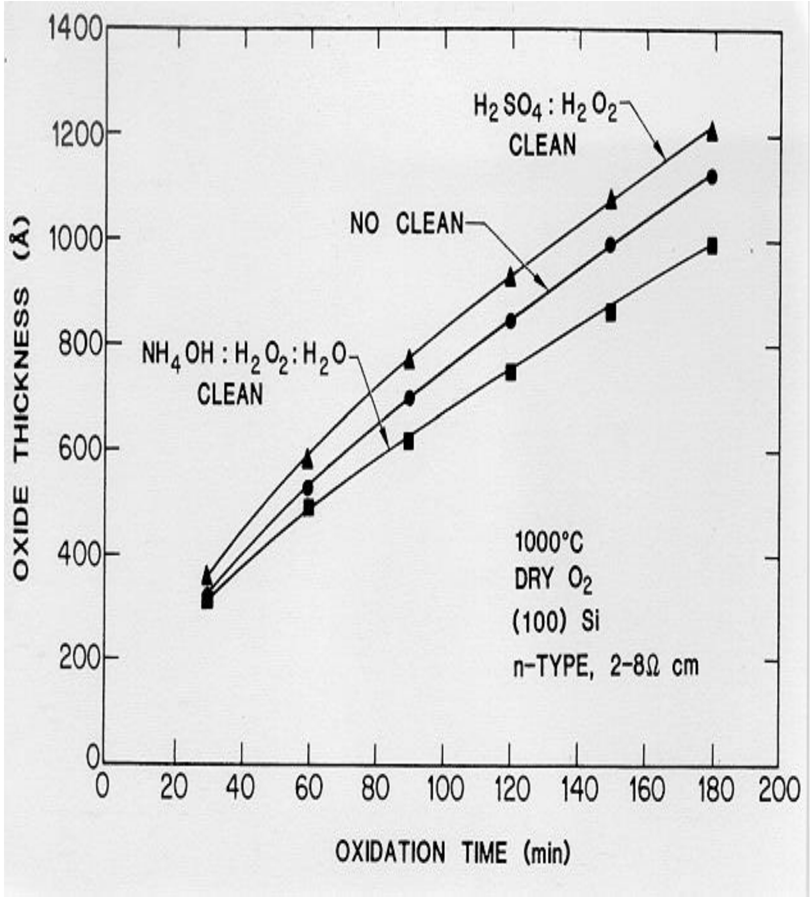
Thermal oxidation

Surface preparation

If the surface is not cleaned uniformly, patches of non-uniform thickness of oxide can be observed.

Pre-oxidation cleaning treatment can affect the subsequent oxidation rate.

Since the treatment incorporating ammonium hydroxide results in the slowest oxidation, it is postulated that an inhibiting nitride layer is formed, which retards the subsequent oxidation process



Influence of cleanliness for oxidation

Thermal oxidation

Properties of thermal SiO_2 and Si

	Si	**SiO_2**
Molecular weight	28.09	60.08
Molecules/cm^3	$5*10^{22}$	$2.3*10^{22}$
Structure	diamond	amorphous
Density (g/cm^3)	2.33	2.21
Energy gap (eV)	1.11	---
Melting point (°C)	1420	1700
Lin. Coeff. Expansion	$2.33*10^{-6}$	$0.5*10^{-6}$
E-modulus (GPa)	120-170	69
Dielectric constant	11.8	3.9
Refractive index	3.4	1.462

Thermal oxidation

Key variables in oxidation

- Temperature
    - Reaction rate
    - Solid state diffusion
- Oxidizing species
    - Wet oxidation is much faster than dry oxidation
    - Dry oxidation gives the better quality in electricial properties
- Surface cleanliness
    - Metallic contamination can catalyzing reaction
    - Quality of oxide grown
- Substrate orientation
    - SiO_2 grows 1.7 times faster on (111) than on (100) surfaces

Annealing

- **Thermal annealing**

  - under N_2

  - under N_2 and H_2

- **Rapid annealing**

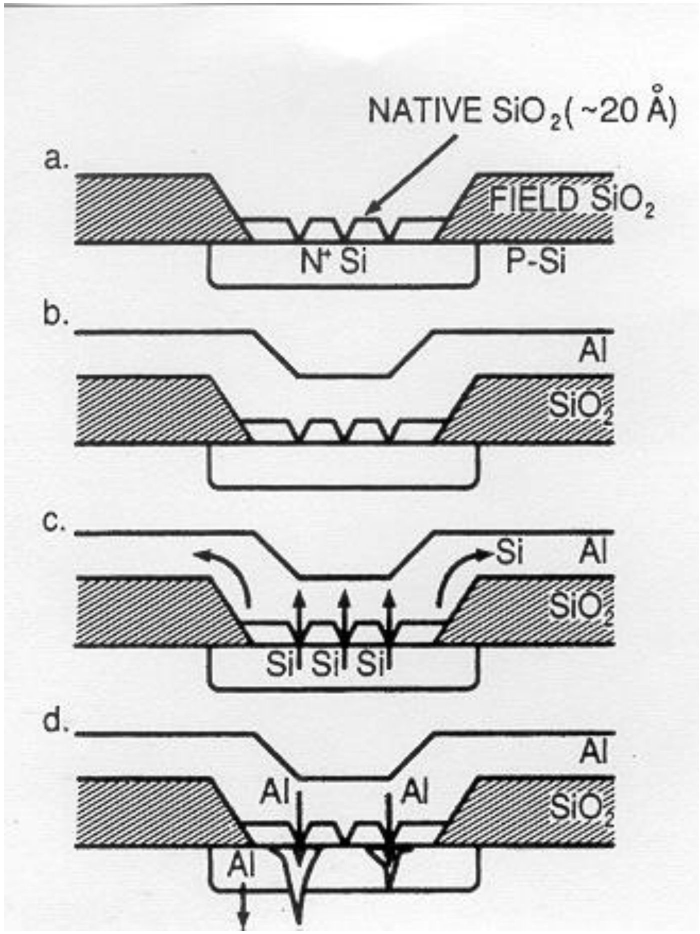
  - pulsed laser (1ps)

  - pulsed electron ion beam

Annealing

Annealing of Al-Si junction

- The goal is to form a ohmic contact between Si and Al.
- Processing of deposited Al films for contacts includes a 450°C heat treatment for 30 min under N_2.
- This enables the Al to reduce the thin native insulating SiO_2 film sinter to Si, thereby lowering the contact resistance



Annealing

Junction spiking

$$b \cong 2\sqrt{D \cdot t} \cdot \left(\frac{H \cdot Z}{A} \right) \cdot S \cdot \left(\frac{\rho_{Al}}{\rho_{Si}} \right)$$

D: diffusion coefficient

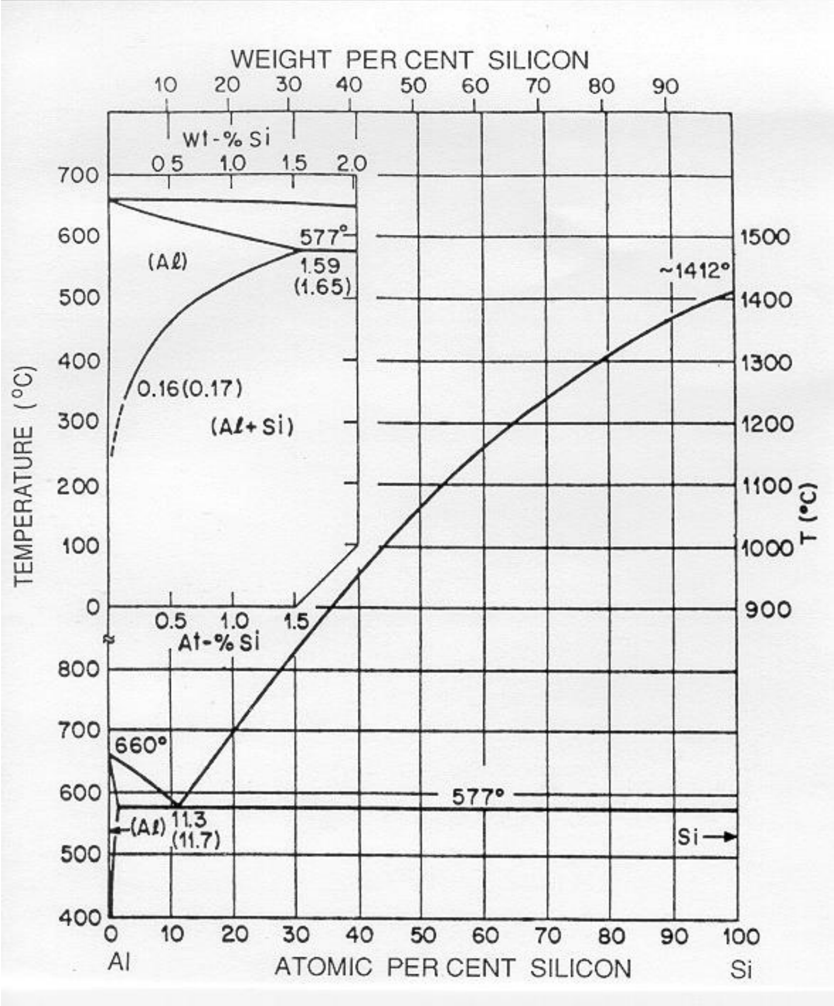
S: solubility

H,Z,A: geometry

r: density

t: time

b: depth into Silicon



Phase diagram of Al-Si system

Annealing

Example

T=500°C, t=30 min

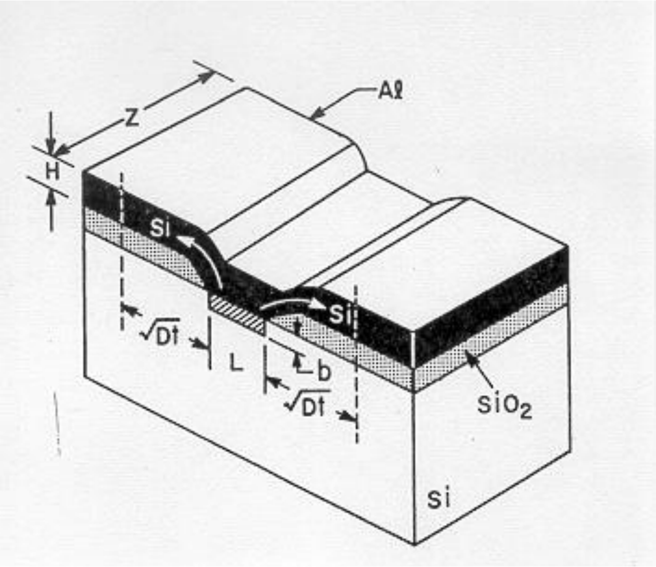
$$b \cong 2\sqrt{D \cdot t} \cdot \left(\frac{H \cdot Z}{A}\right) \cdot S \cdot \left(\frac{\rho_{Al}}{\rho_{Si}}\right)$$

$D = 2*10^{-8}\ cm^2/s$

S = 0.8 wt%

H = 1µm, Z = 5 µm, ZL = 16 µm²

$r_{Al}/r_{Si} = 1.16$



Result b= 0.35 µm

Al will fill to a depth of 0.35 µm from which silicon is consumed.

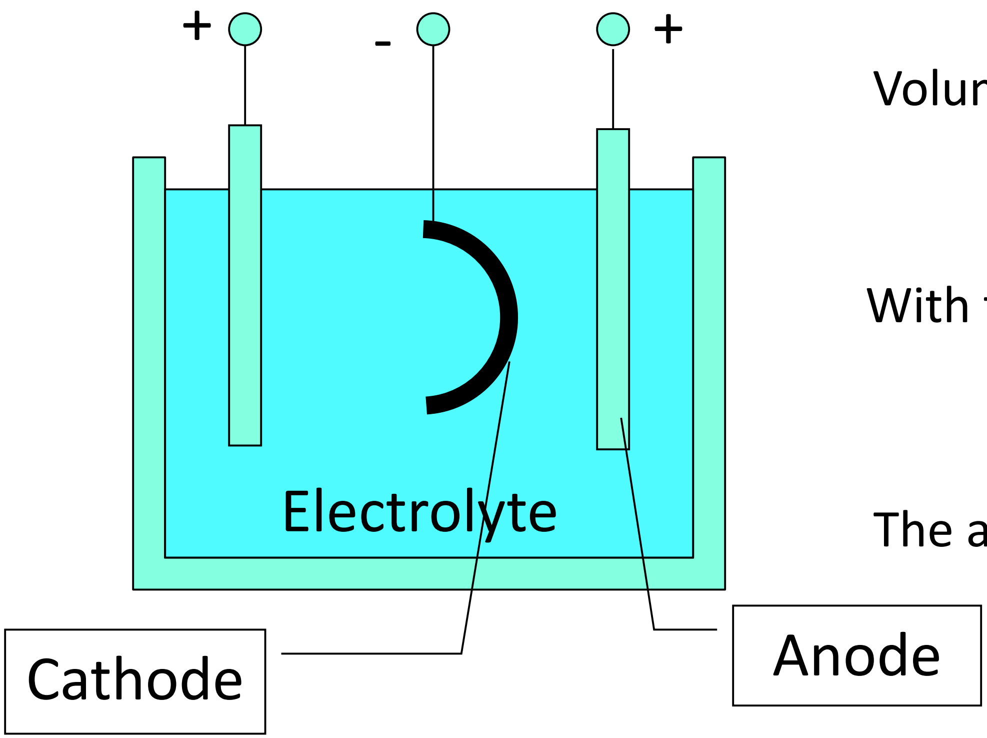
Electrodeposition

- Reasons for Plating:
  - corrosion, appearance, wear resistance, electrical conductivity, solderability & lubricity
  - Inexpensive technique : few material necessary
  - A large number of metals can be electroplated

- Electroplating:
  - coating of a thin metallic layer onto the surface of a substrate by an electrolytic process in which metal ions deposited onto a cathode work material

- « Electroless » deposition:
  - coating of a thin metallic layer onto the surface of a substrate by a chemical reaction

Electrodeposition



Volume of metal plated: $V = CIt$

where C= plating constant

With the cathode efficiency

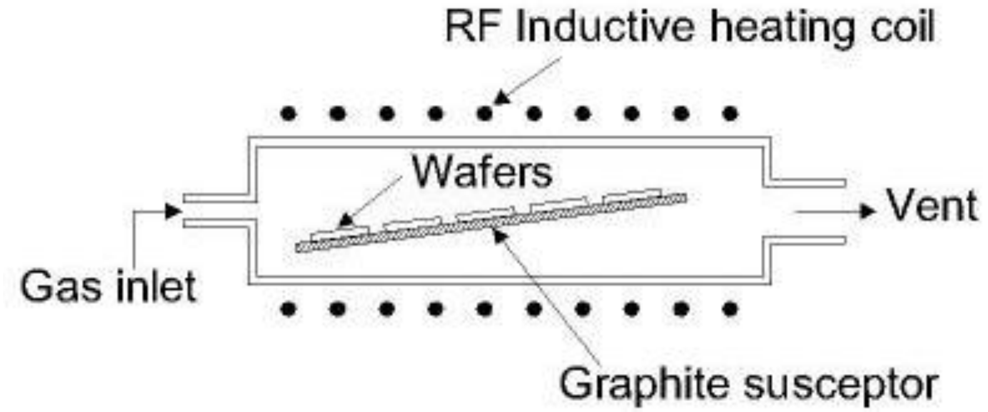
$$V = \eta CIt$$

The average plating thickness

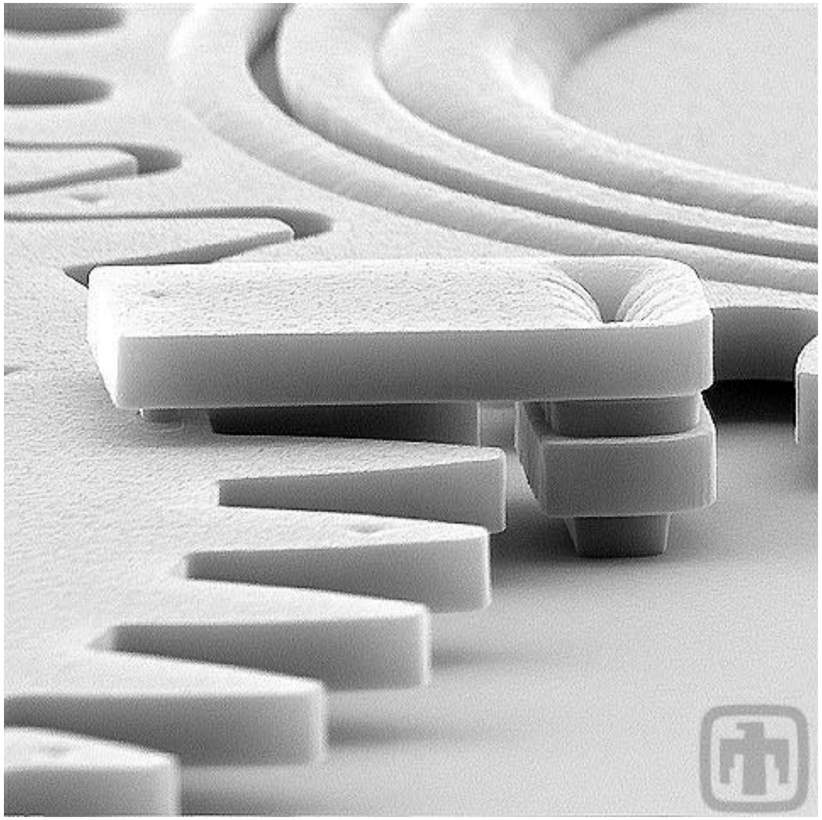
$$d = \frac{V}{A}$$

Epitaxy

This technology is quite similar to what happens in CVD processes, however, if the substrate is an ordered semiconductor crystal (i.e. silicon, gallium arsenide), it is possible with this process to continue building on the substrate with the same crystallographic orientation with the substrate acting as a seed for the deposition. If an amorphous/polycrystalline substrate surface is used, the film will also be amorphous or polycrystalline.



Surface Micromachining – Poly-Si process



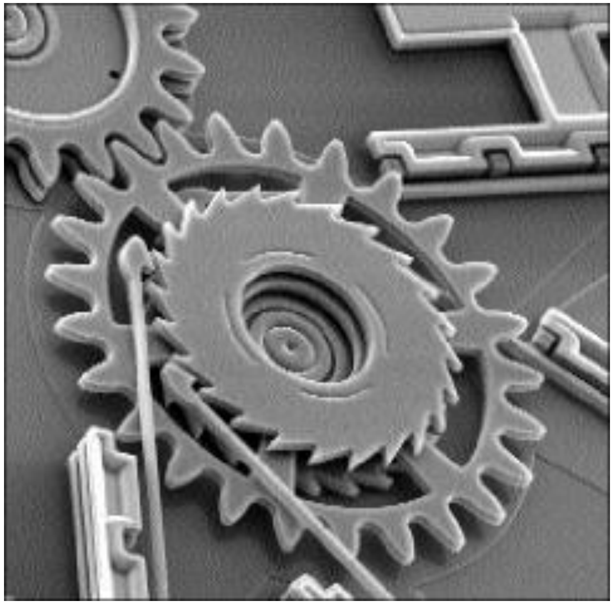
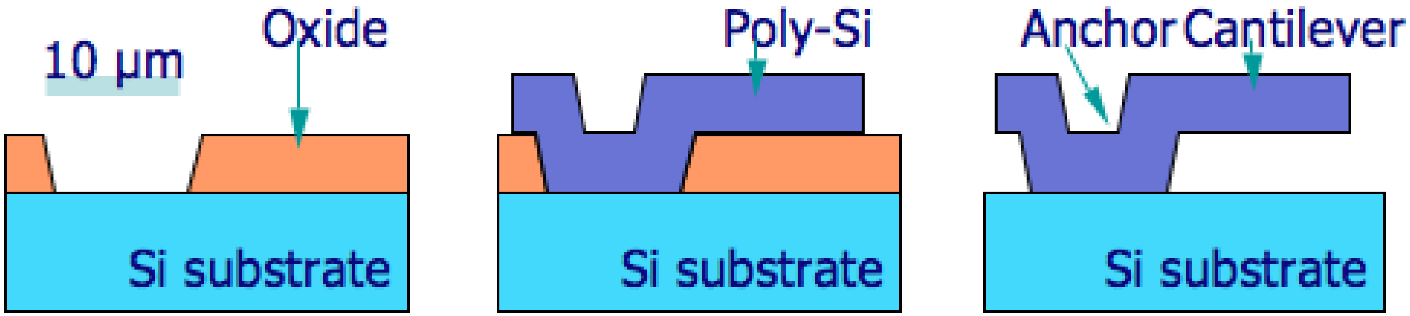


Image source: MEMX.com

Sandia national Labs

Surface Micromachining – Poly-Si process

surface micromachining builds microstructures by deposition and etching of different structural layers on top of the substrate. Generally *polysilicon* is commonly used as one of the layers and *silicon dioxide* is used as a *sacrificial layer* which is removed or etched out to create the necessary void in the thickness direction. Added layers are generally very thin with their size varying from 2-5 Micro meters



Common Material Systems

(1)Poly-Si/Silicon Dioxide

This is the most common material system : LPCVD deposited poly-Si as the structural material and thermally grown or LPCVD deposited oxide as the sacrificial material. The oxide is readily dissolved in HF without the poly-Si being affected.

Advantages :

•Both materials are used in IC processing and, therefore, their deposition technologies are readily available.

•Poly-Si has excellent mechanical properties and can be doped for various electrical applications.

•The oxide can be thermally grown and CVD deposited at a wide temperature range (~ 200 °C to ~ 1200 °C) which is very useful for various processing requirements.

•The material system is compatible with IC processing.

Together with this material system silicon nitride is often used for electrical insulation.

Common Material Systems

(2) Silicon Nitride/Poly-Si

Here LPCVD silicon nitride is used as the structural material, whereas poly-Si is the sacrificial material.
In this case Si anisotropic etchants such as KOH andEDP are used to dissolve poly-Si.

(3) Tungsten/Silicon Dioxide

CVD deposited tungsten is used as the structural material with the oxide as the sacrificial material. HF is used for removing the oxide.

Common Material Systems

(4) Polyimide/Aluminum

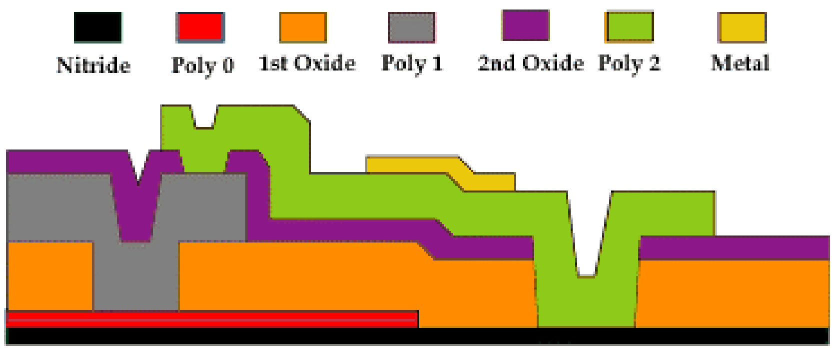
Polyimide is the structural material and aluminum is the sacrificial material. Acid-based aluminum etchants are used to dissolve the aluminum sacrificial material.

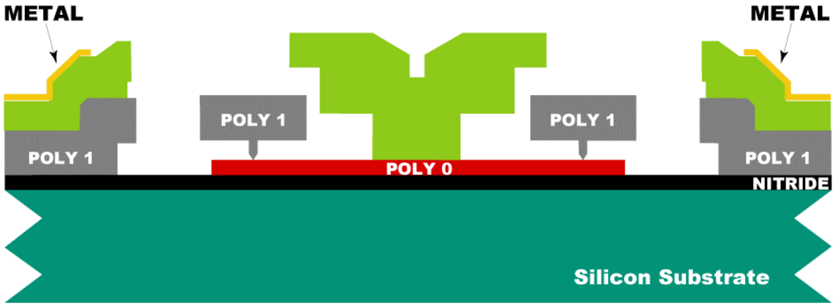
Advantages :

•Polyimide has a small elastic modulus which is ~ 50 times smaller than that of poly-Si.
•Polyimide can take large strains before fracture.
•Both polyimide and aluminum can be prepared at low temperatures (< 400 °C).
•A disadvantage of polyimide is its viscoelastic characteristics; it creeps.

MUMPS Process

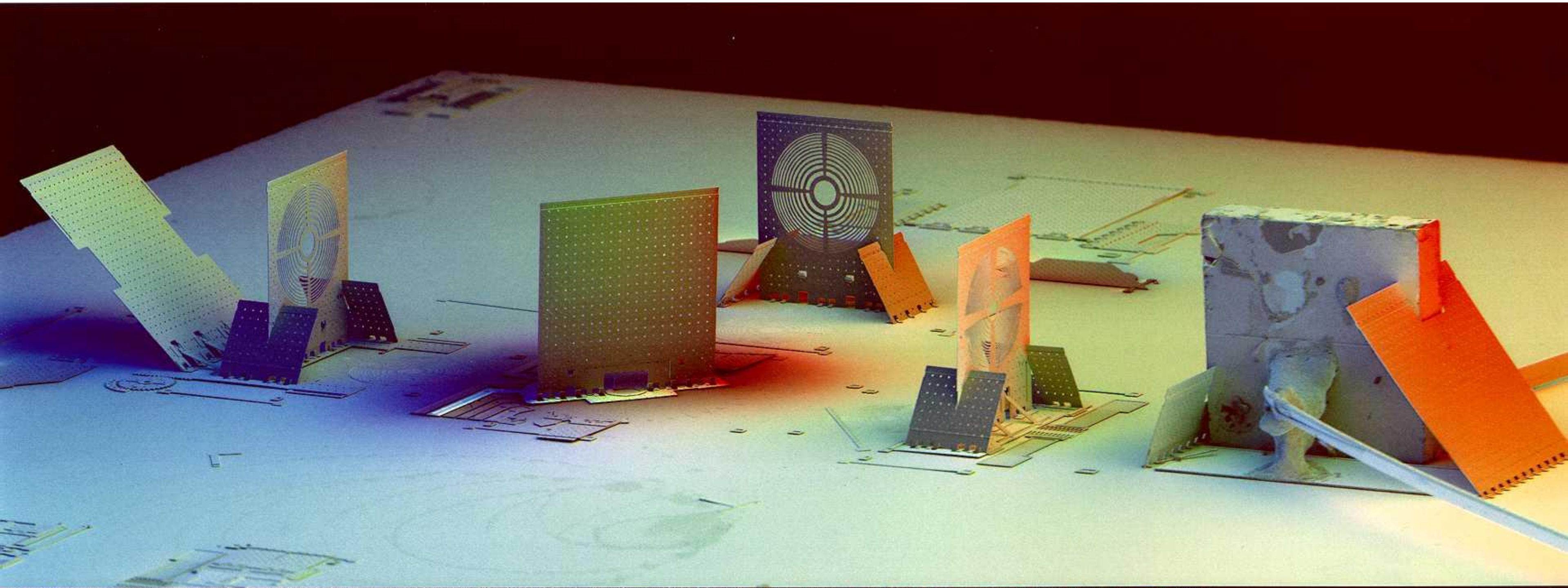
The Multi-User MEMS Processes or MUMPs™ is a commercial program that provides the international industrial, governmental and academic communities with cost-effective, proof-of-concept surface micromachining fabrication. MUMPs™ is designed for general purpose micromachining by outside users who would like to fabricate MEMS devices





http://web.nchu.edu.tw/~daw/Teaching/MEMS/Handouts/mumps-short.pdf

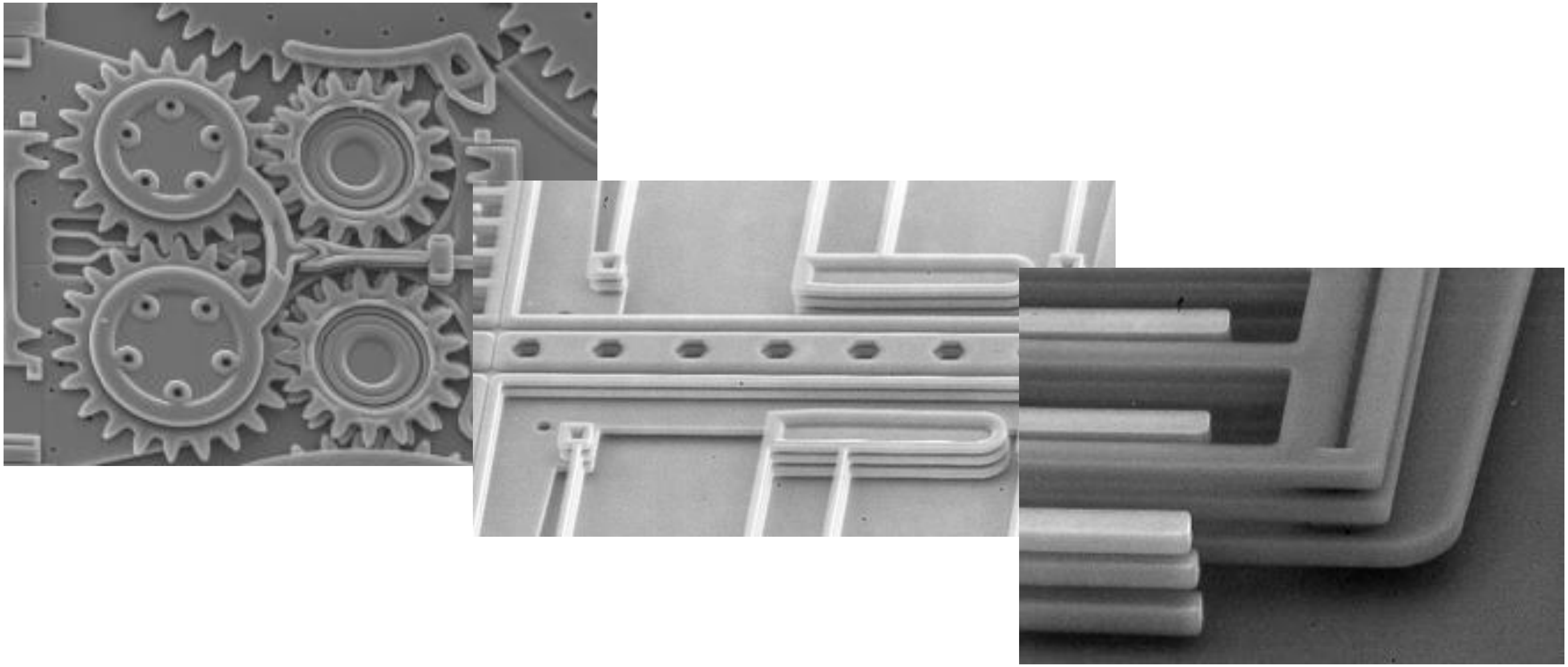
MUMPS Process



Micro Optics (laser, 3 fresnel lenses, beam splitter, & 45 deg. mirror) Nano-fabrication Micromachining (Fabricated by Ming Wu, L. Y. Lin, J. L. Shen, S. S. Lee, and C. R. King @ U.C.L.A. , E.E. Dept.)
50X @ 4"x5" size. © David Scharf, 1996. All rights reserved. (9605-009a)

Summit-V Process

Sandia Ultra-planar, Multi-level MEMS Technology 5 (SUMMiT V^{TM}) Fabrication Process is a five-layer polycrystalline silicon surface micromachining process (one ground plane/electrical interconnect layer and four mechanical layers).



Sandia labs

- Hot Embossing
- XeF2 Dry Phase Etching
- Electro-Discharge Micromachining
- Laser Micromachining
- Focused Ion Beam Micromachining
- Wafer bonding (adressed in the lecture on packaging)

1. **Introduction**
   – Cleanroom facilities
   – Silicon bulk material
2. **Lithography**
   – E-Beam
   – Pattern transfer
3. **Bulk Micromachining**
   – Isotropic wet etching
   – Anisotropic wet etching (KOH),
   – Isotropic Dry etching (RIE)
   – Anisotropic Dry etching (DRIE)
4. **Surface Micromachining**
   – Thin film depositions techniques, PVD, CVD, electroplating, …
   – Poly-SI, sacrificial layer techniques
5. **Other techniques**